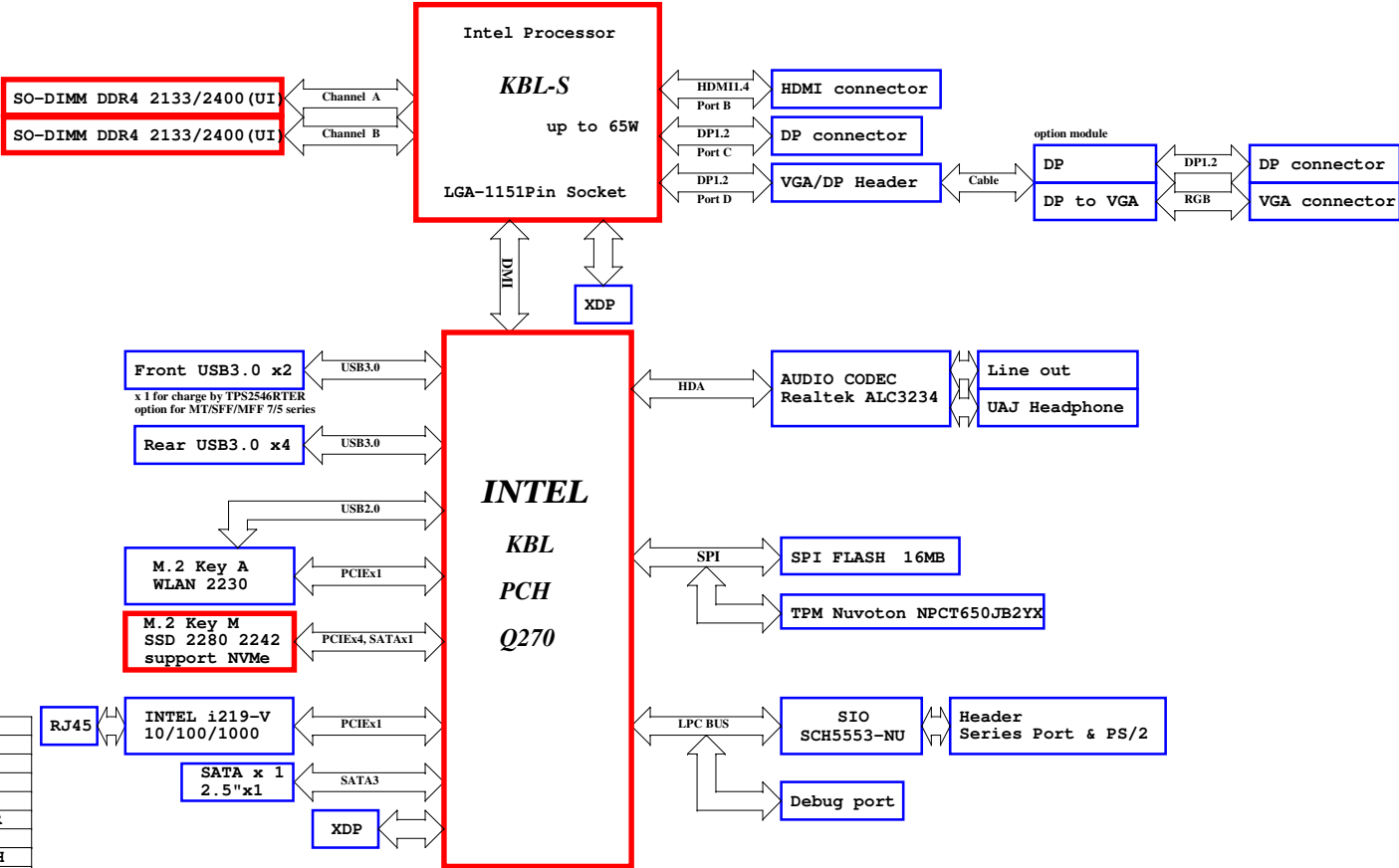


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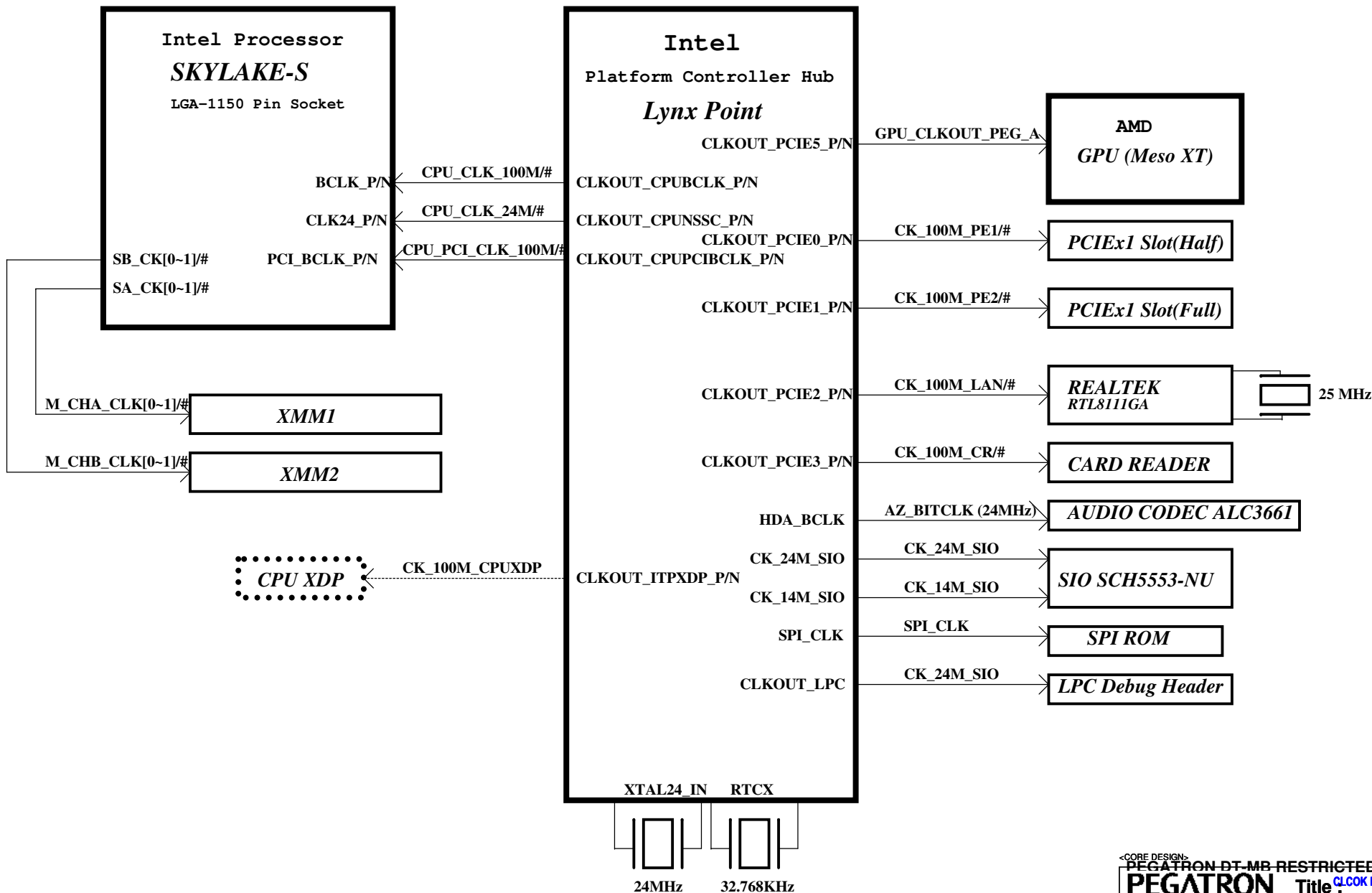
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01	BLOCK DIAGRAM
02	CLOCKS DISTRIBUTION
03	SIGNAL & RESET MAP
04	CHANGE HISTORY
05	POWER FLOW 35W
06	POWER DISTRIBUTION
07	POWER SEQUENCE
08~13	CPU LGA1151
14	DDR4 SODIMM CH-A
15	DDR4 SODIMM CH-B
16	DDR4 TERMINATION A&B
17~24	INTEL PCH
25	SM BUS Control
26	SPI ROM
27	ME DISABLE
28	NGFF KEY A 2230 (WLAN)
29	NGFF KEY M 2280 (SSD)
30	LOM Intel i219
31	LAN JACK
32	N/A
33	Front USB3.0
34	N/A
35	Front 3.0 USB CHARGE IC
36	REAR USB3.0
37	REAR USB3.0
38	N/A
39	TYPE-C CYPD2122
40	TYPE-C CONN
41	PS2 and Comport header
42	VGA option header
43	REAR LINE OUT& GHS CONN
44	N/A
45	SIO SCH5555V-NU
46	SCREW HOLE
47	FAN CIRCUIT
48	intruder
49	DEBUG LED
50	APS/LPC DEBUG
51	RTC
52	SATA HDD CONN & LED
53	HDMI OUT
54	AUDIO CODEC ALC3234
55	PWRBTN & LED
56	N/A
57	N/A
58	TPM Z32H320TC
59	TPM NPCT650JAAYX
60	DP CONN
63~64	DC IN
65	PCHPWROK_VCCSTPG
68	VCCSA & VCCIO
69	5VSB/+5VA/+3P3VA
70	+3P3VSB/WLAN

Revision: A00

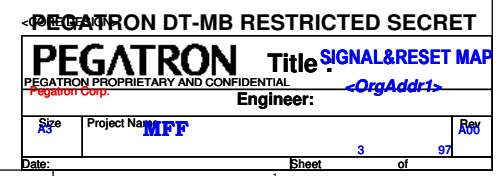


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title: BLOCK DIAGRAM	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer: <OrgAddress>		Rev: 1	
Size	Project Name	Engineer	Rev
UMK			



ONBOARD POWER CHIP or MOS SOCKET or SLOT



Schematics Change History

[illegible]

PEGATRON DT-MB RESTRICTED SECRET

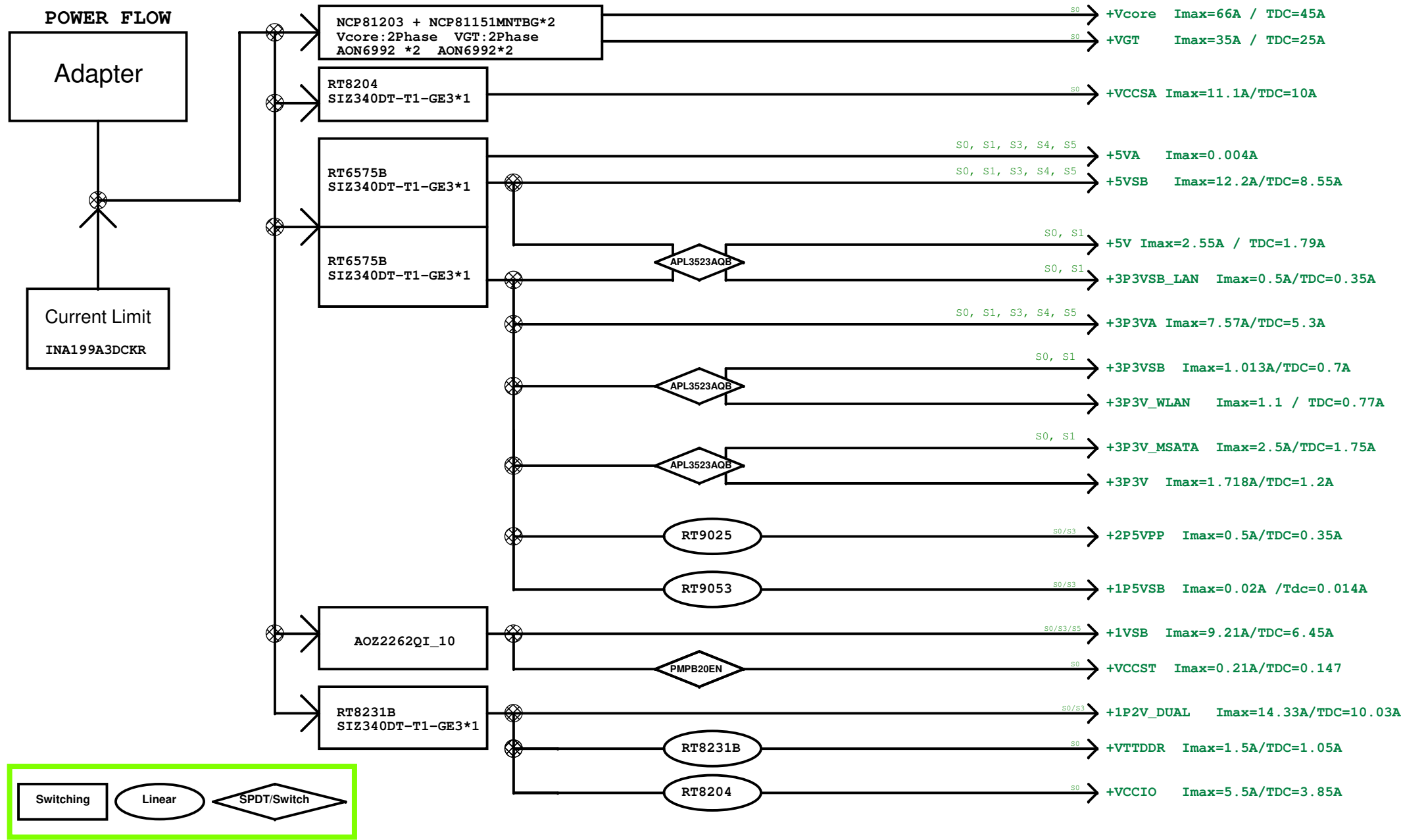
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Pegatron Proprietary and Confidential
 Pegatron Corp. Engineer: <OrgAddr1>

Size A3	Project Name MFF	Rev A00
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Date: _____ Sheet 4 of 97

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+VCORE	CPU SKYLAKE-S
+1P05V_SA (+VCCSA)	-> 70A - 65W
+V_GT (+VCCGT)	-> 11. 1A
+0P95V_CPUIO (+VCCIO)	-> 35A
+1V_ST (+VCCST)	-> 5. 5A
+1P2V_DUAL (VDDQ)	-> 0.06A+0. 15A
+1P2V_DUAL (VDDQ)	-> 2. 8A+0. 13A
VCCST_PWRGD (VCCSTG)	-> 0.02A

	PCH Lynx Point
+1VSB	-> 7. 11A
+3P3V	-> 0. 007A
+3P3VSB	-> 0. 74A
+3P3VA	-> 0. 2A
+BATT	-> 0.001A

	DDR4
+1P2V_DUAL	-> 9. 51A
+VTT_DDR	-> 0. 75A

	Panel (HD)
+3P3V	eDP to LVDS IC (S1U1)-> 2A
+3P3V	eDP to LVDS EEPROM (S1U2)-> 0.003A
+5V_LCD	-> 1. 2A

+3P3V	DP
	DP Conn (125)-> 0. 5A

+3P3V	HDMI
	HDMI-Redriver (MU1)-> 0. 2A
+5V_HDMI	HDMI-Out Conn (J137)-> 0. 5A

+3P3VSB_LAN	LAN IC
	LAN IC (LU1)-> 0. 3A

+3V_WLAN	WLAN
	WLAN (J218)-> 2A

+3P3V	M. 2
	M. 2 (J1)-> 2. 5A

+3P3VSB	CARD READER
	CR IC (U3)-> 1. 6A - 5. 28W
CR_3V3	CR CONN (J2)-> 0. 8A-2. 64 W

+3P3VSB	ALC3224 Codec
	-> 12mA - 39. 6mW
+5VSB	-> mA
+3P3V	-> 12mA - 39. 6mW

+5V_FAN	CPU FAN (P70)
	-> 0. 9A -8. 4 W

+5VSB	ODD & HDD
	HDD-> 1A - 5W
	ODD-> 2A - 10W

+5VSB	USB PORTS
	Charge IC -> 2. 5A
+5VSB_CHARGING	SIDE USB3.0 (J221) -> 2A
+5VDUAL_WAKE	SIDE USB3.0 (J212) -> 0. 9A
+5VDUAL_WAKE	REAR USB3.0 x2 (J226) -> 1. 8A
+5VDUAL_WAKE	REAR USB2.0 x2 (J210) -> 1A

+3P3VSB	WEBCAM
	-> 0. 5A

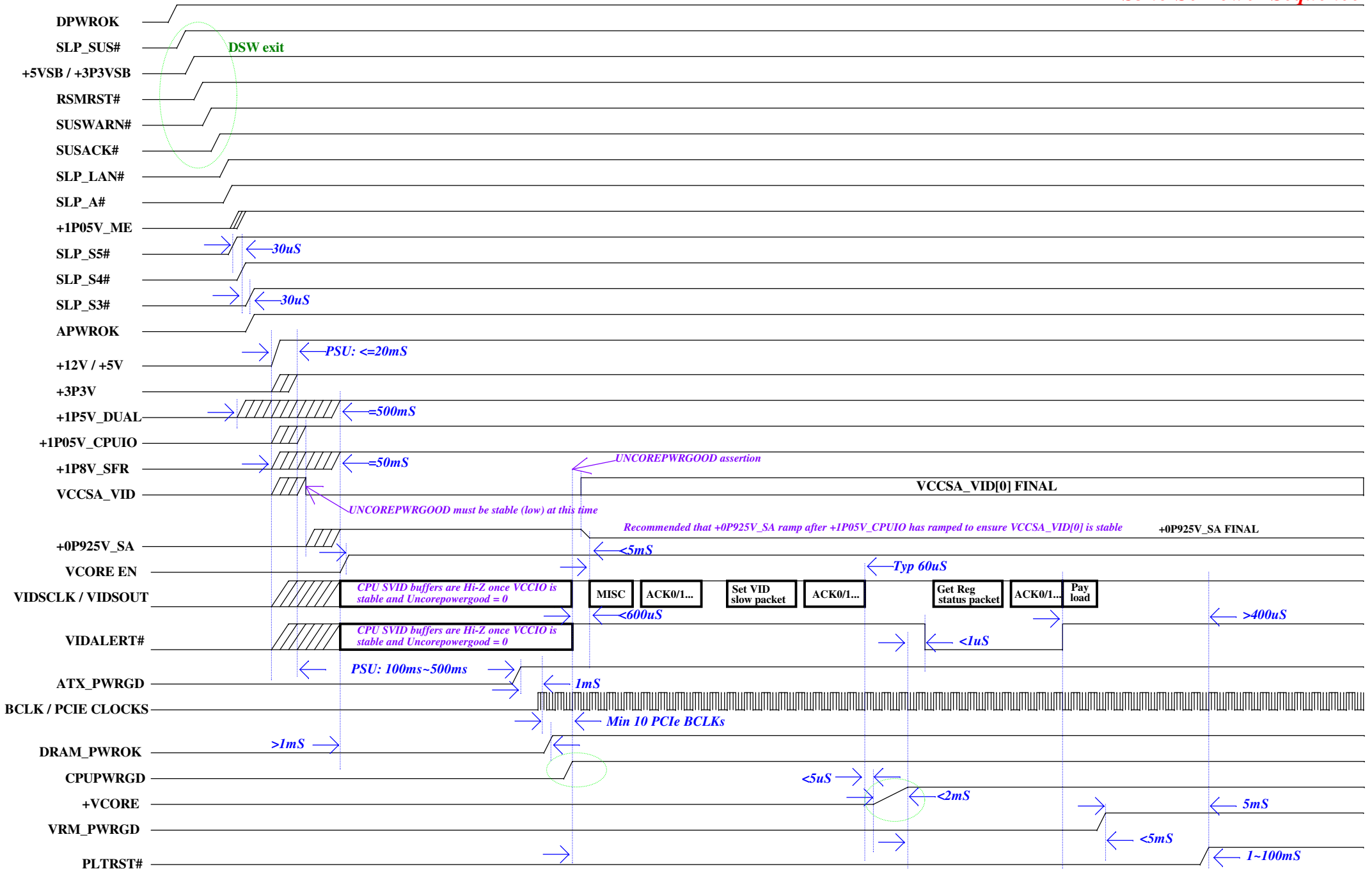
+5VDUAL_WAKE	TOUCH
	-> 0. 5A

+3P3V	SIO SMSC5555
	-> 1mA - 3. 3mW
+3P3VA	-> 11mA - 36. 3mW
+3P3VSB	-> 500mA - 1. 65W
+BATT	-> 1mA - mW

+3P3V	TPM
	TPM-> 1mA
+3P3VSB	TPM-> 0. 3A

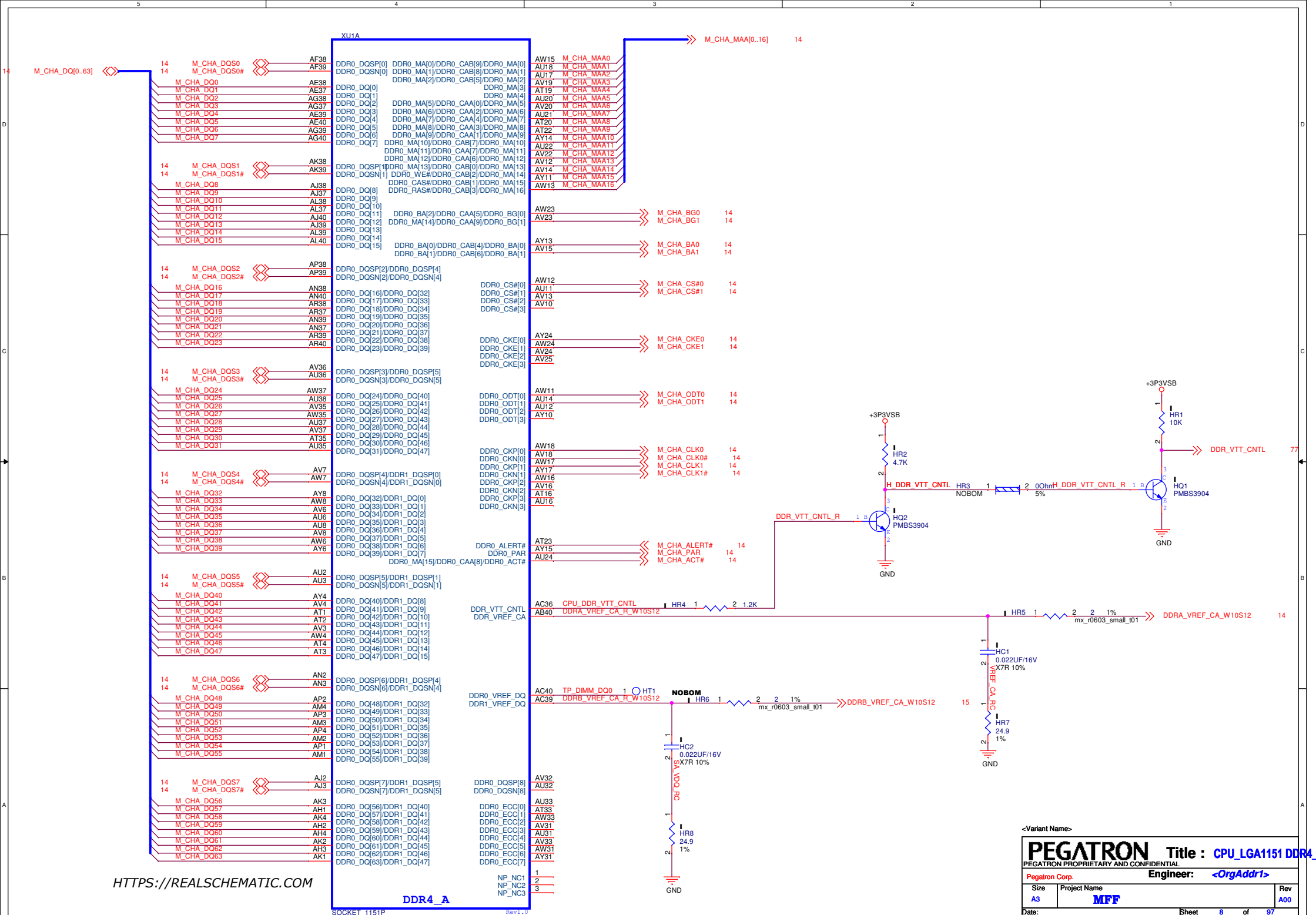
+3P3VSB	SPI
	-> 50mA - 165mW

S5 to S0 Power Sequence



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PEGATRON DT-MB RESTRICTED SECRET
POWER SEQUENCE
 PEGATRON PROPRIETARY AND CONFIDENTIAL
 PEGATRON Corp. Engineer: <OrgAddr1>
 Size Project Name: **MFF** Rev
 Date: Sheet 7 of 97



15 M_CHB_DQ[0..63]

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M_CHB_DQ1
M_CHB_DQ2
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XU1B_1

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AJ7
AE6
AF7
AH7
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AE7
AF6

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DDR1_DQSN[0]/DDR0_DQSN[2]
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DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]

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DDR1_DQ[21]/DDR0_DQ[53]
DDR1_DQ[22]/DDR0_DQ[54]
DDR1_DQ[23]/DDR0_DQ[55]

DDR1_DQSP[3]/DDR0_DQSP[7]
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DDR1_DQ[31]/DDR0_DQ[63]
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M_CHB_BG0 15
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M_CHB_BA0 15
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M_CHB_CS#0 15
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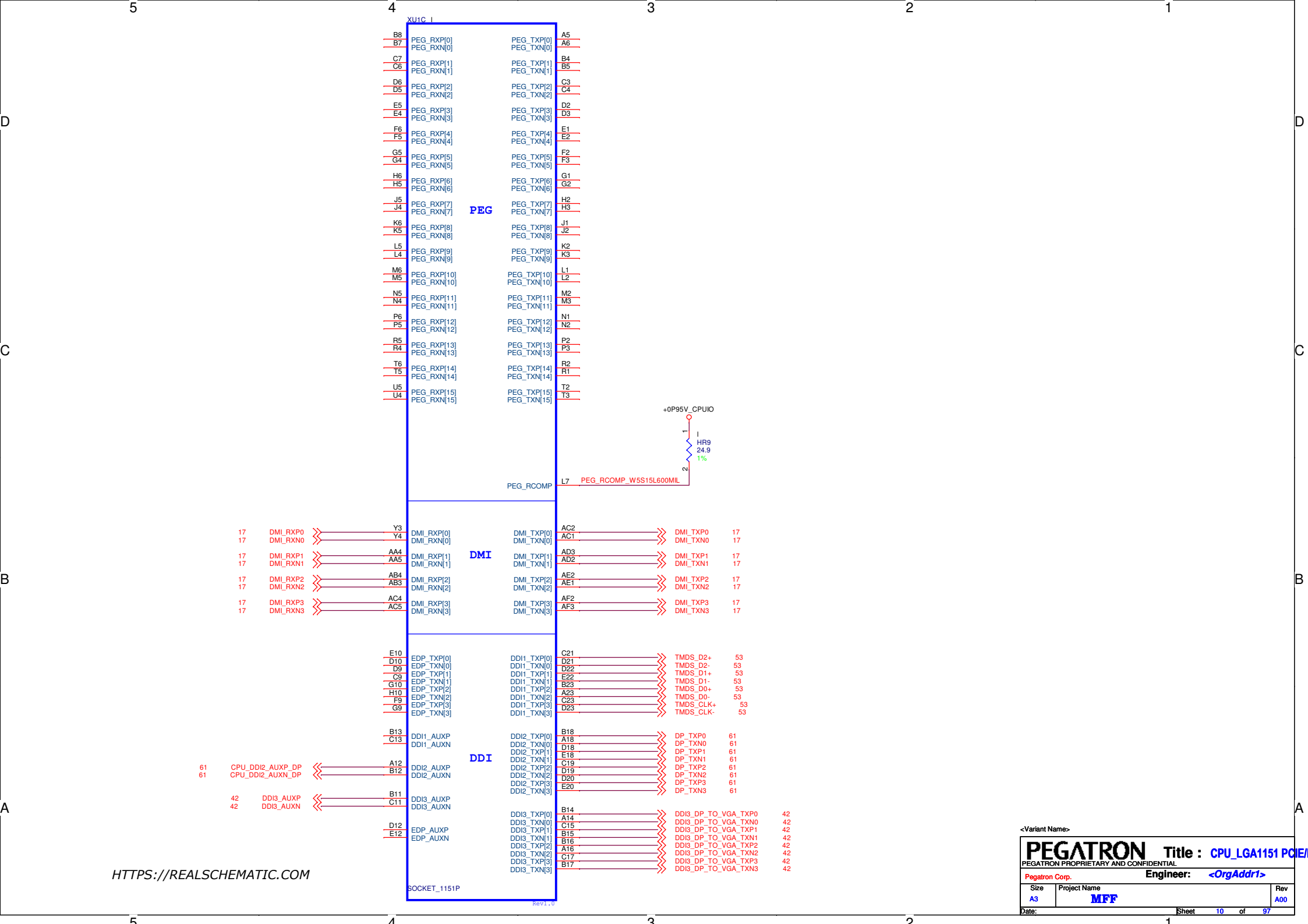
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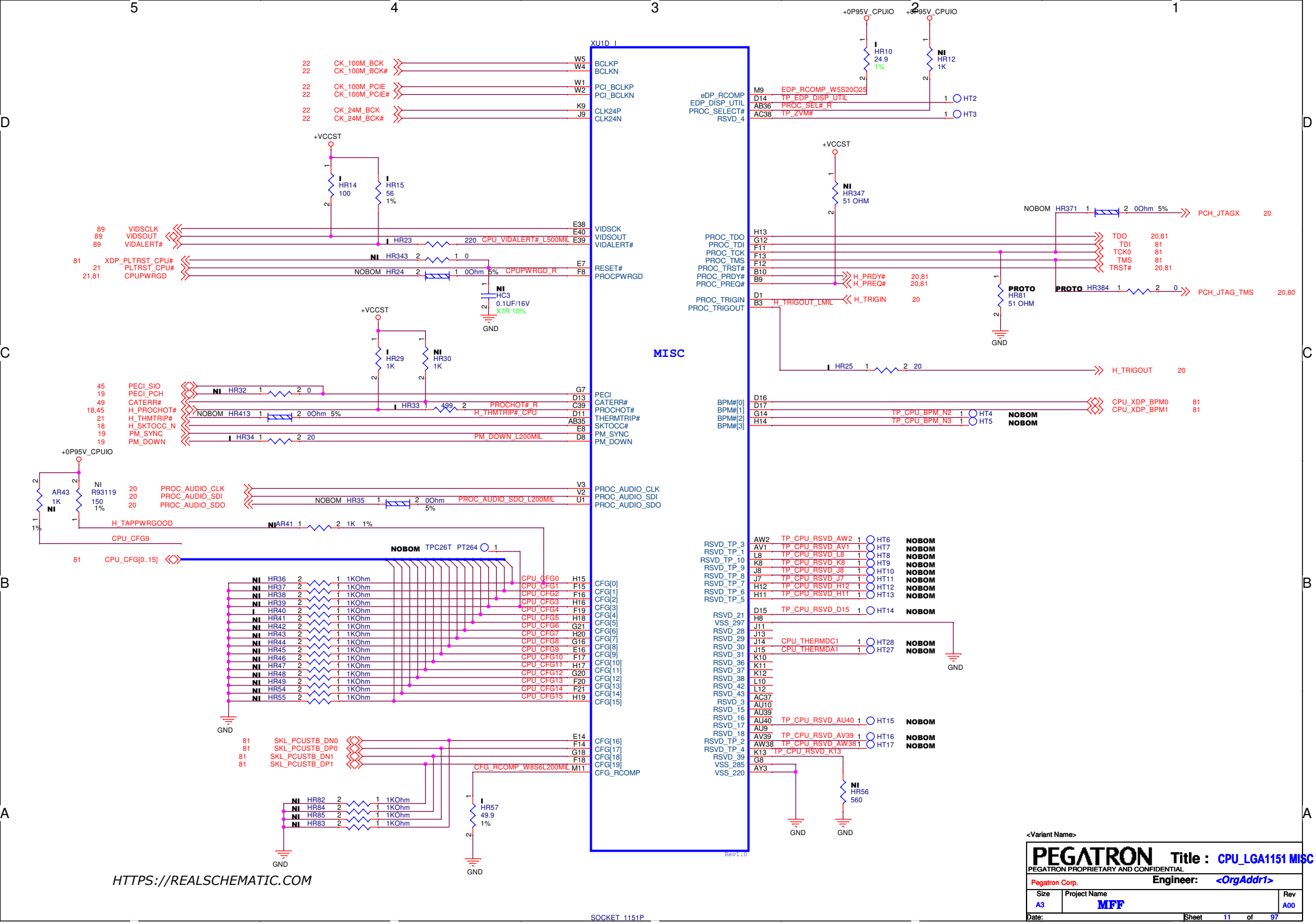
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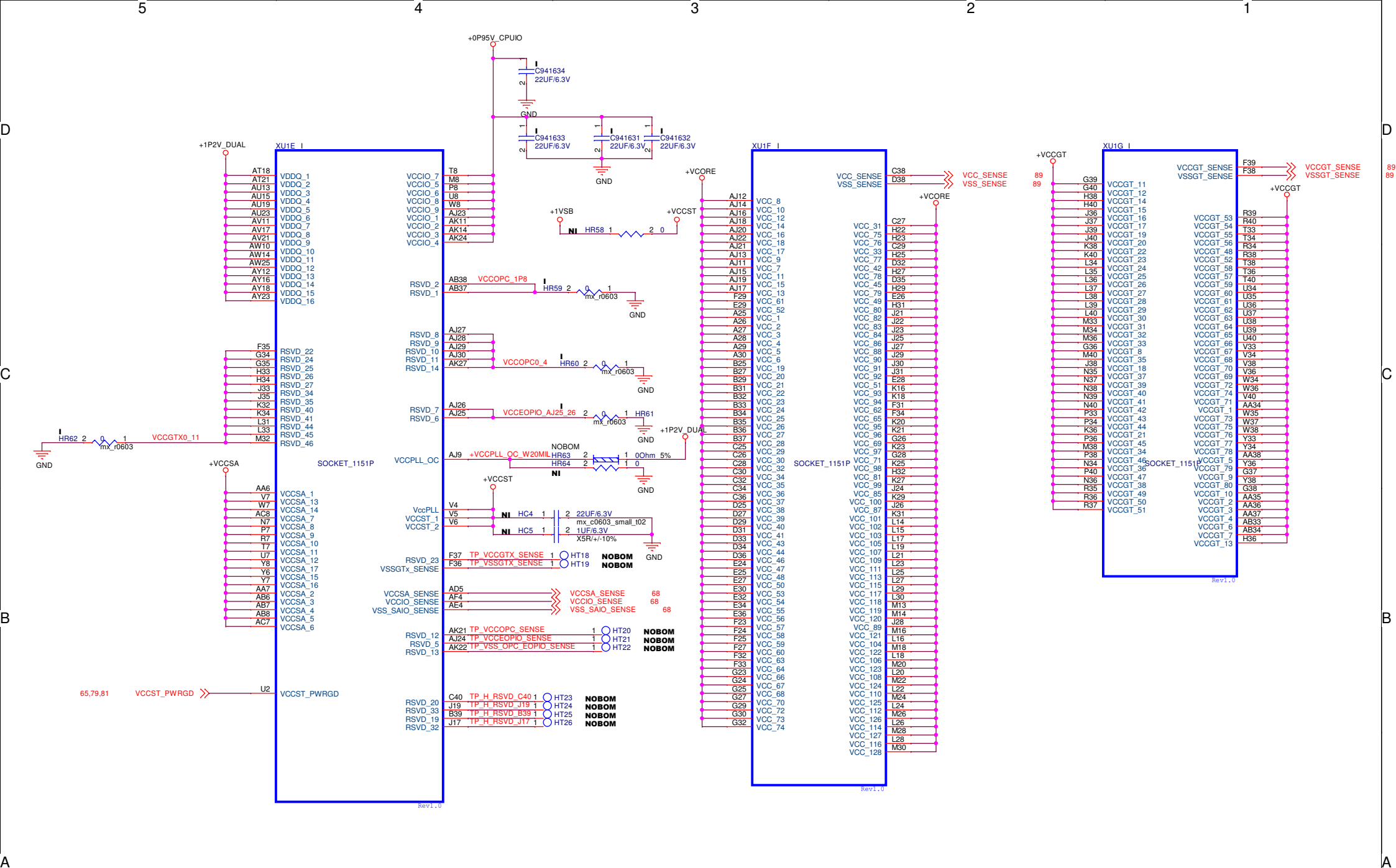
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Pegatron Corp. Engineer: <OrgAddr1>

Size	Project Name	Rev
A3	MFF	A00
Date:	Sheet	9 of 97







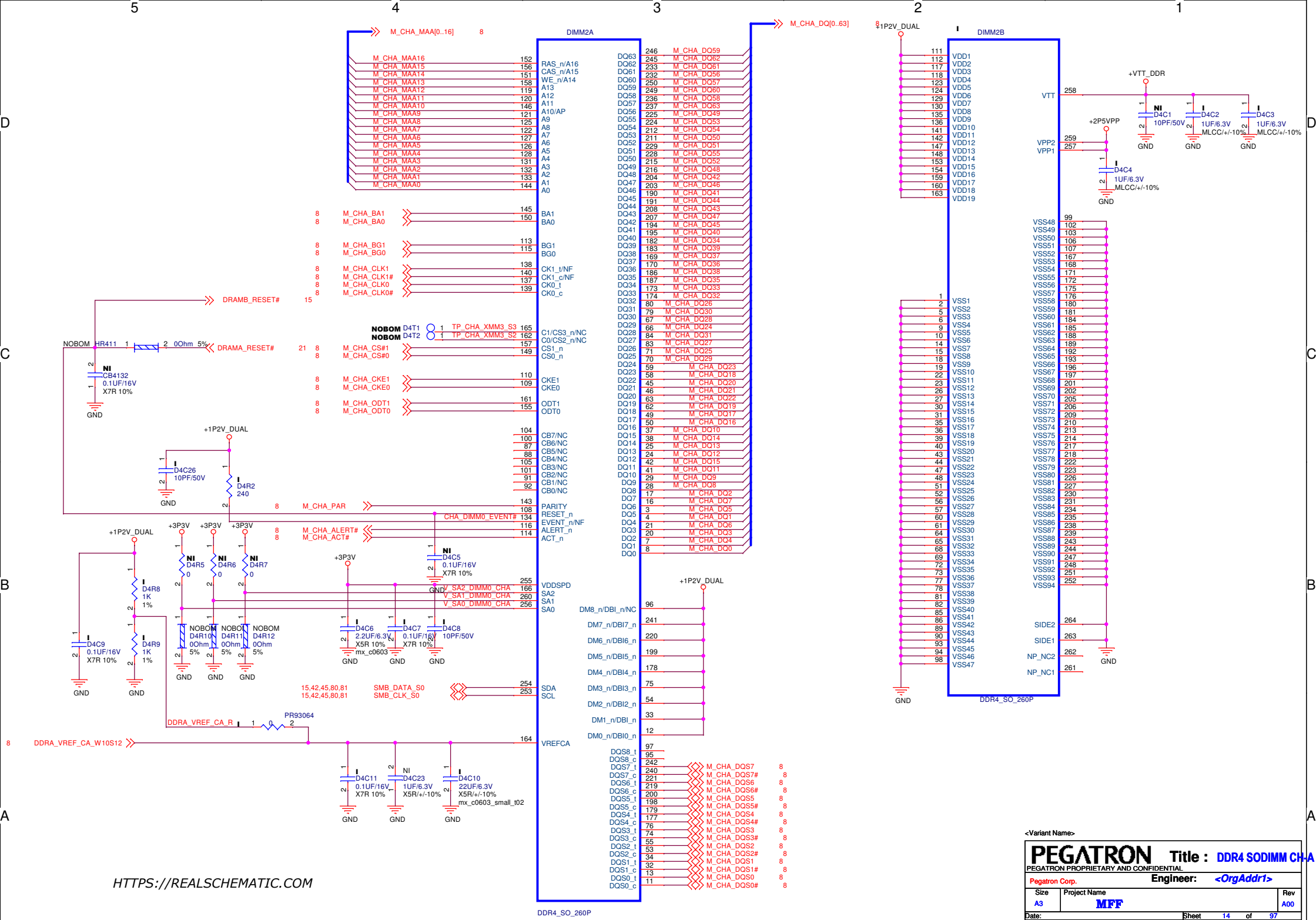
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PEGATRON PROPRIETARY AND CONFIDENTIAL

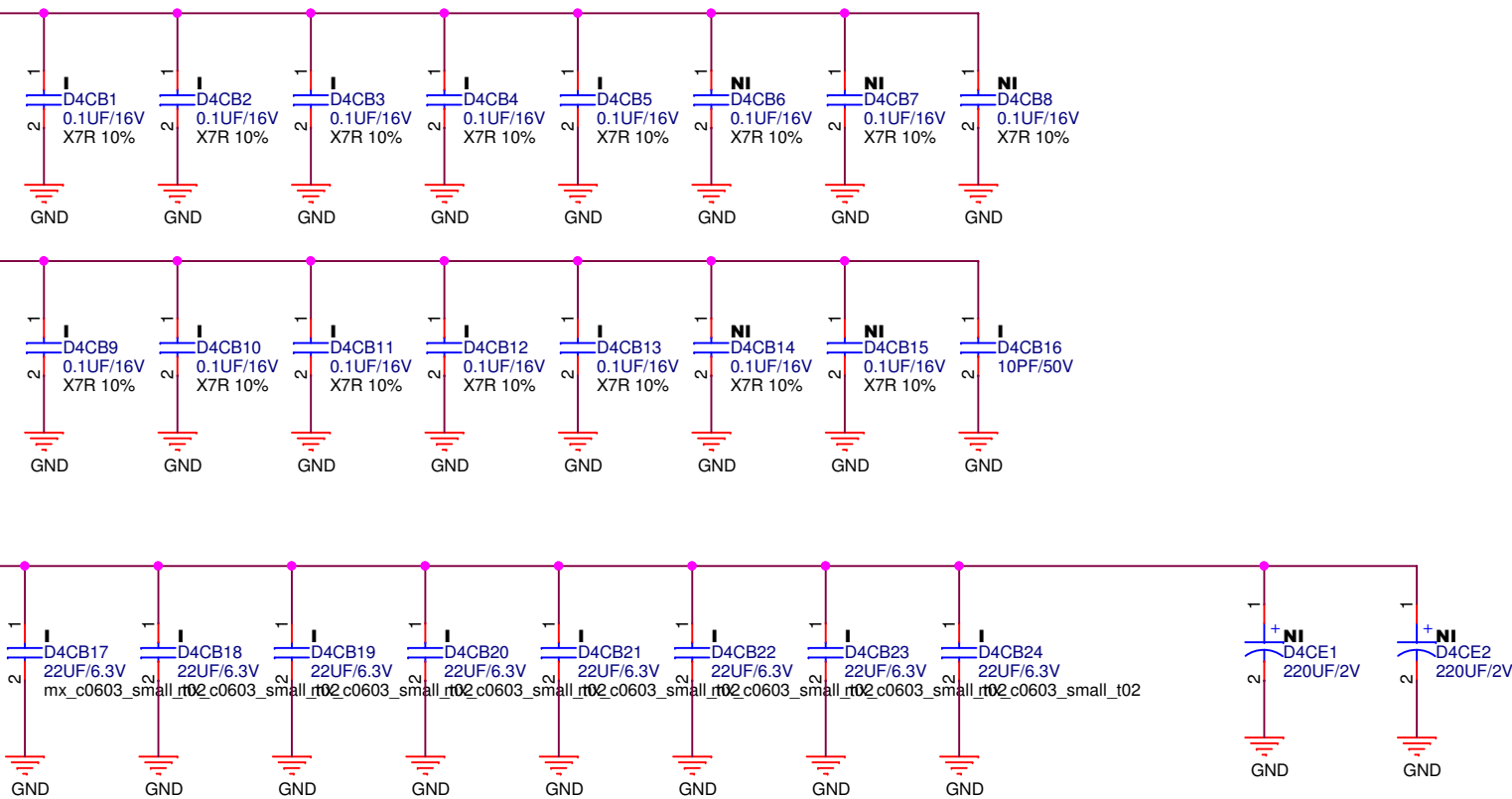
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Size	Project Name	Rev
A3	MFF	A00

Date: Sheet 12 of 97



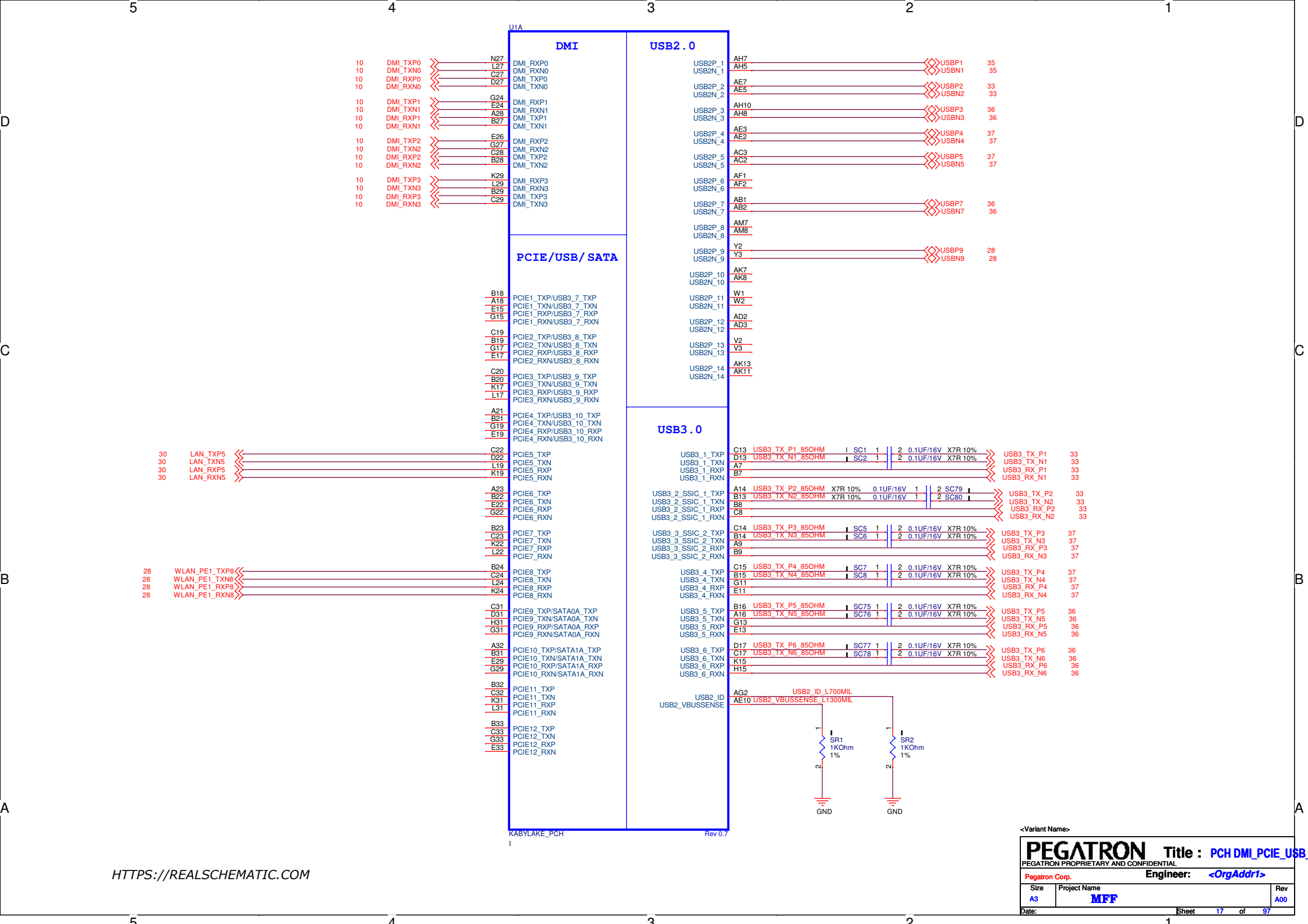
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Size	Project Name		Rev
A4	MFF		A00
Date:		Sheet	16 of 97

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<Variant Name>

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PEGATRON PROPRIETARY AND CONFIDENTIAL

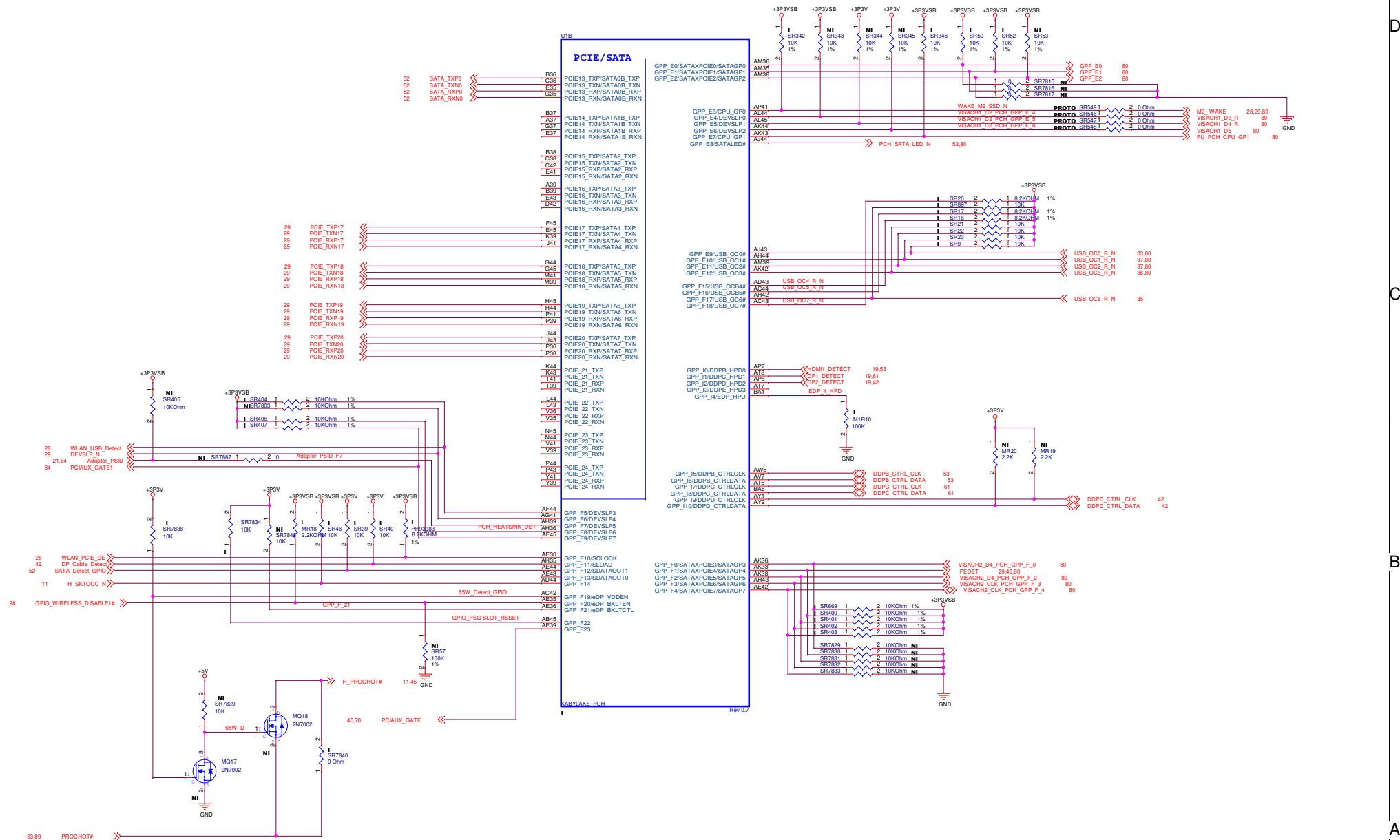
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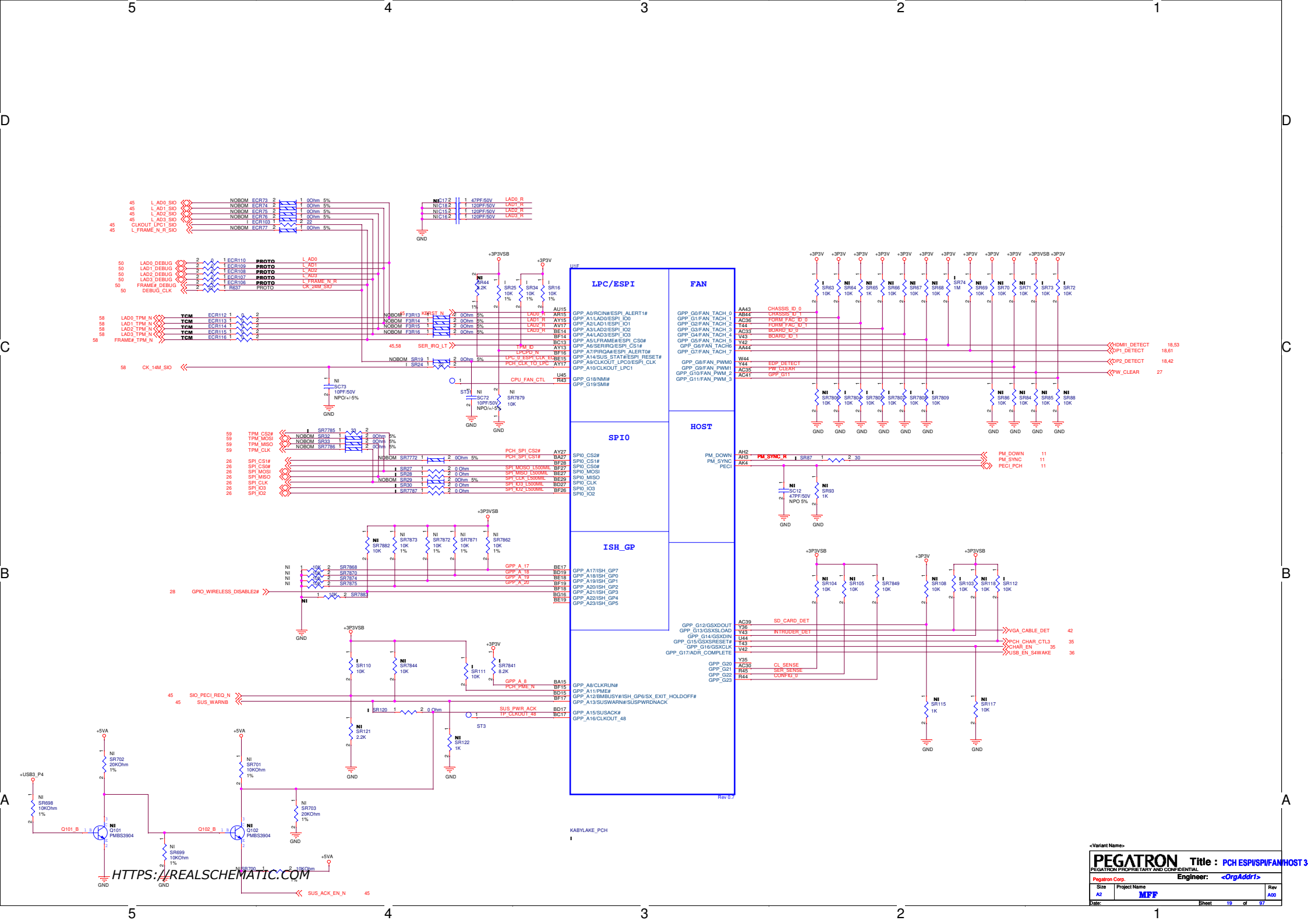
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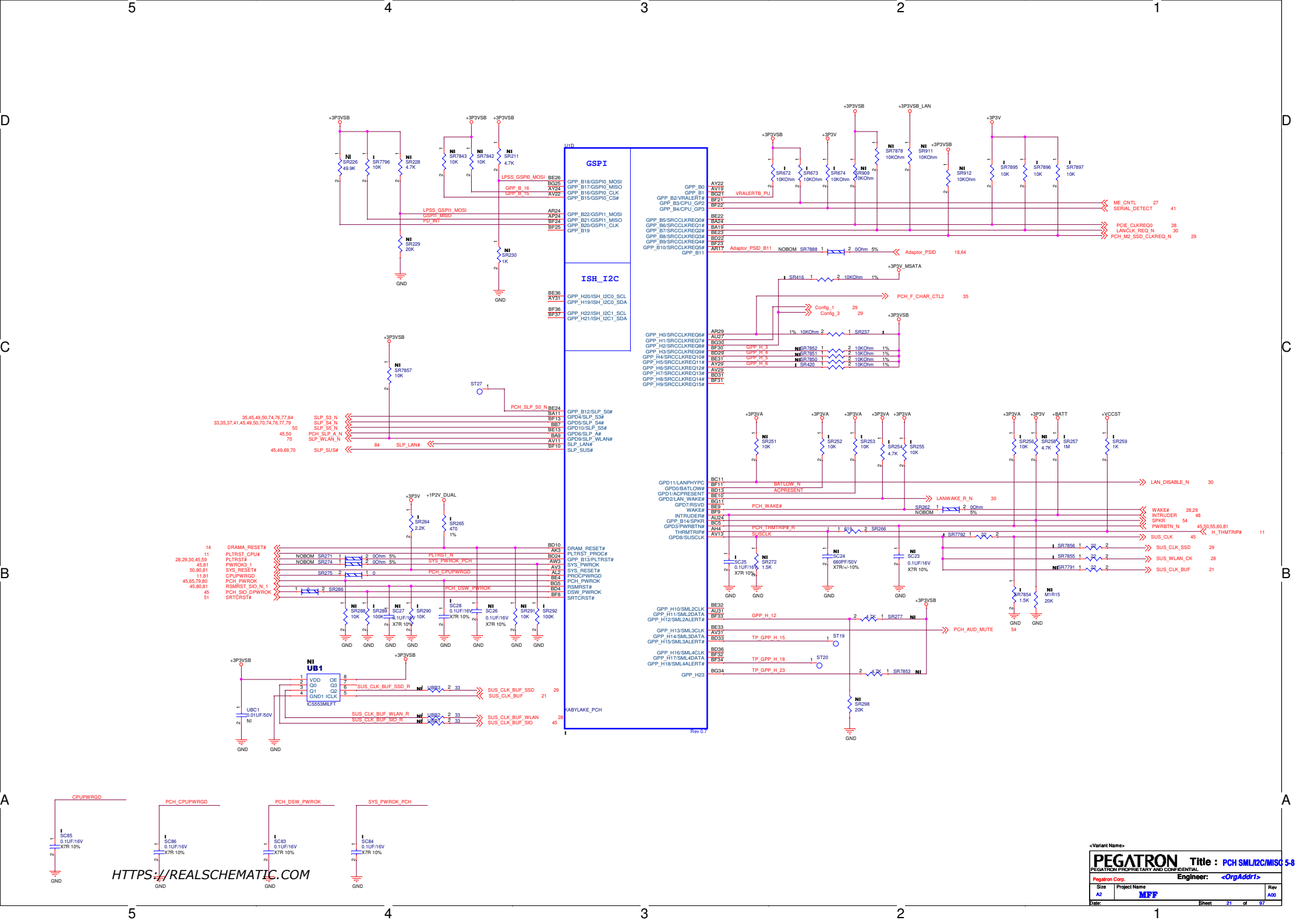
A3 MFF

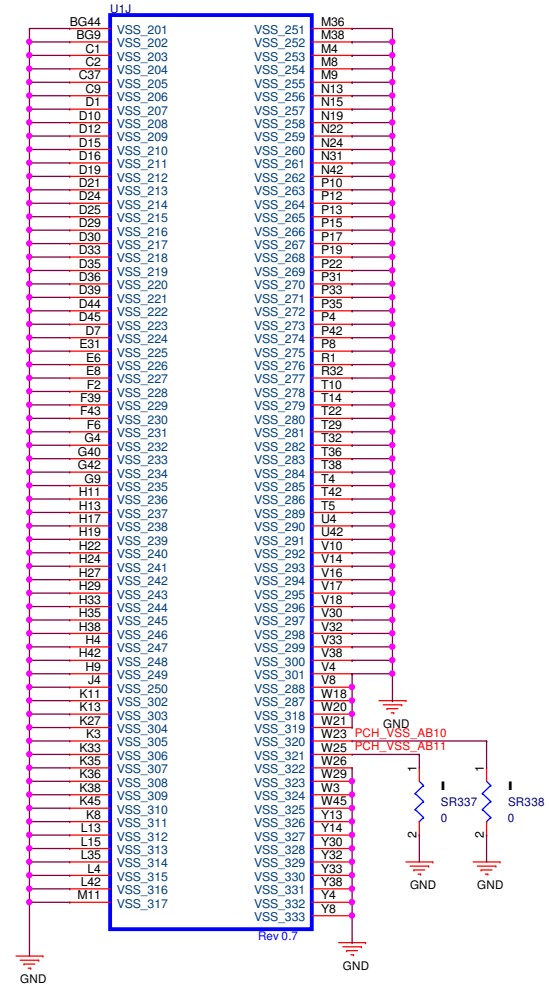
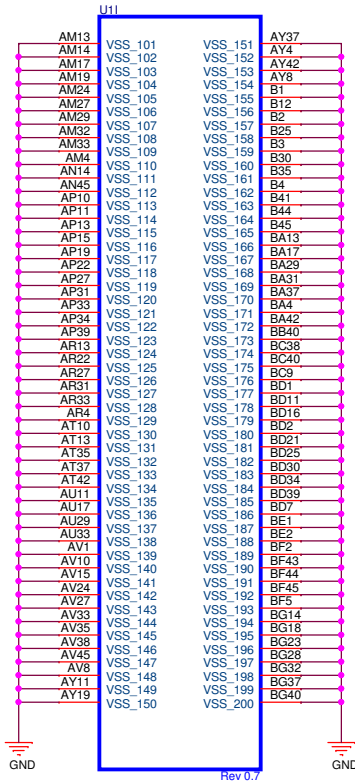
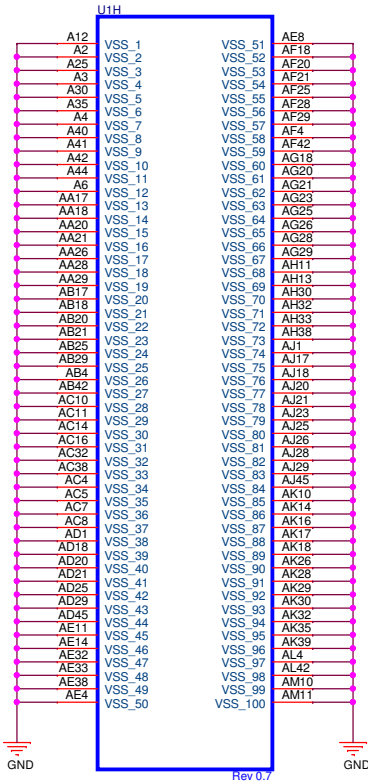
Date: Sheet 17 of 97

Rev A00









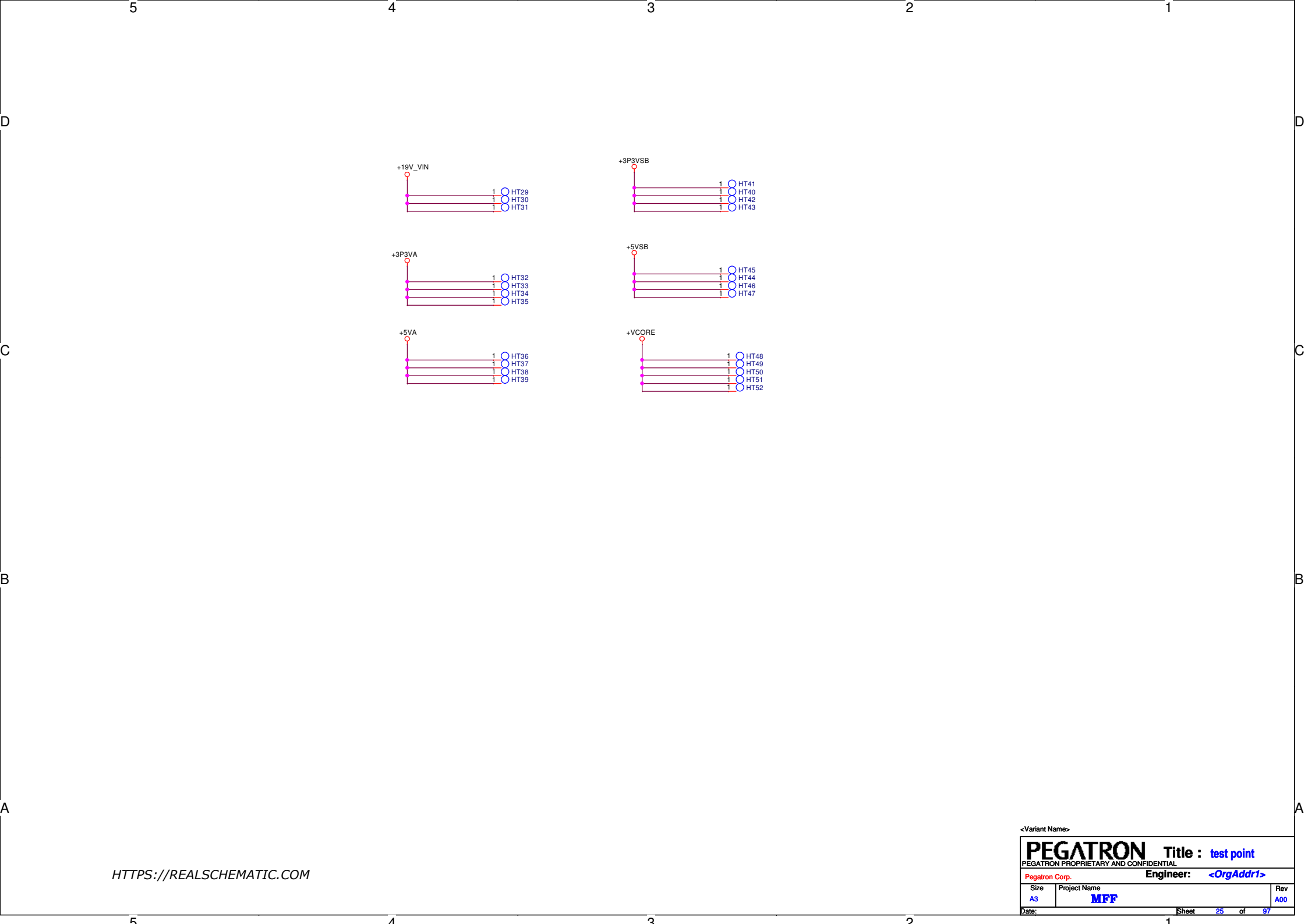
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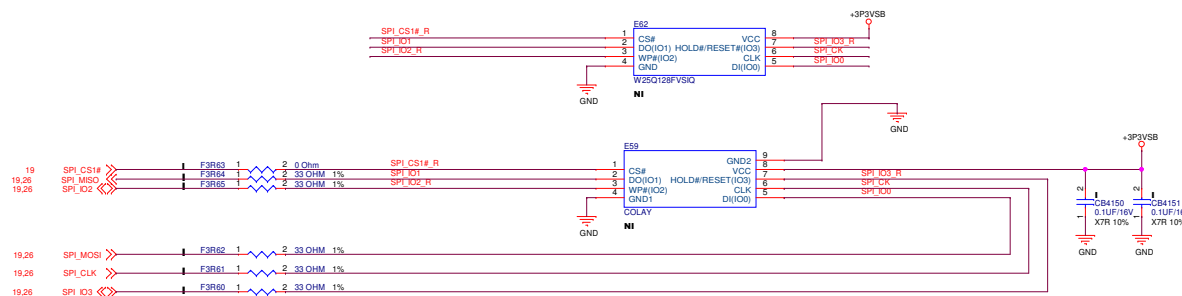
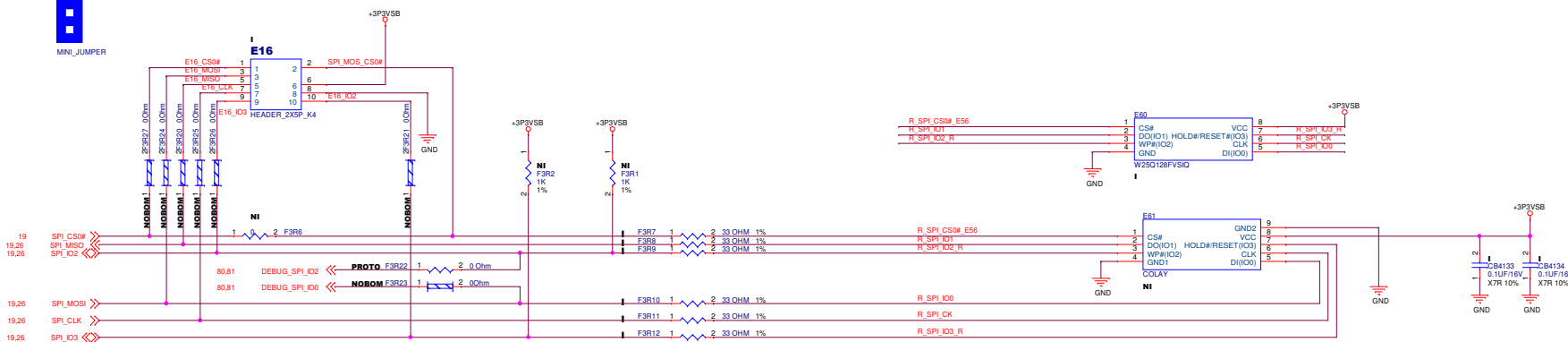
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PEGATRON PROPRIETARY AND CONFIDENTIAL

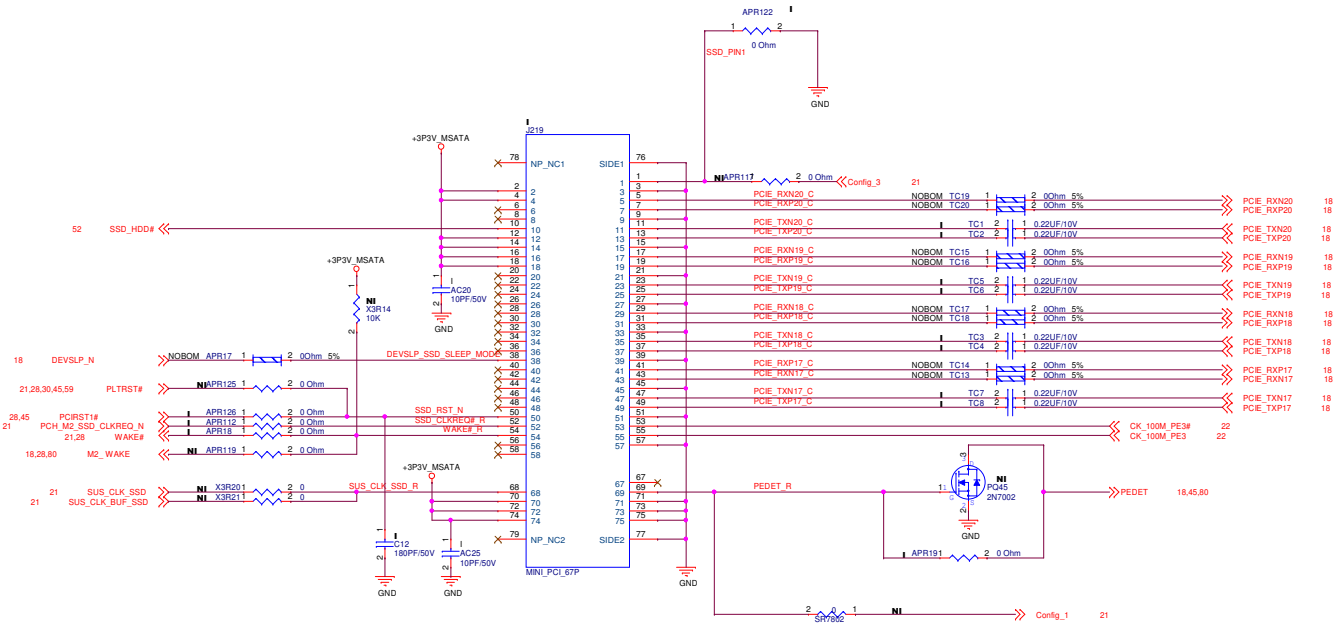
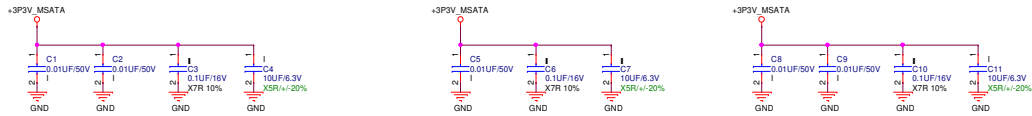
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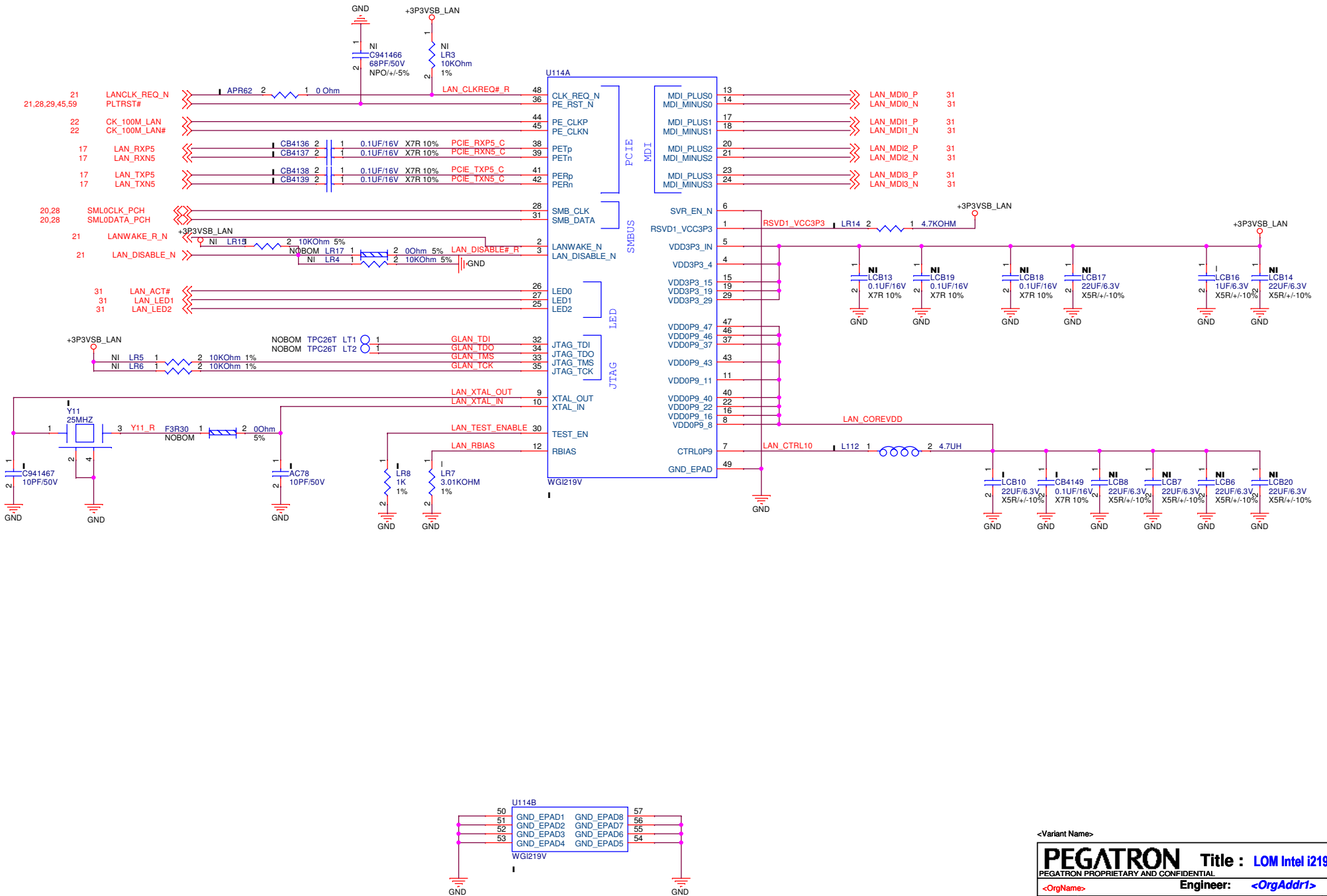
Size	Project Name	Rev
A3	MFF	A00

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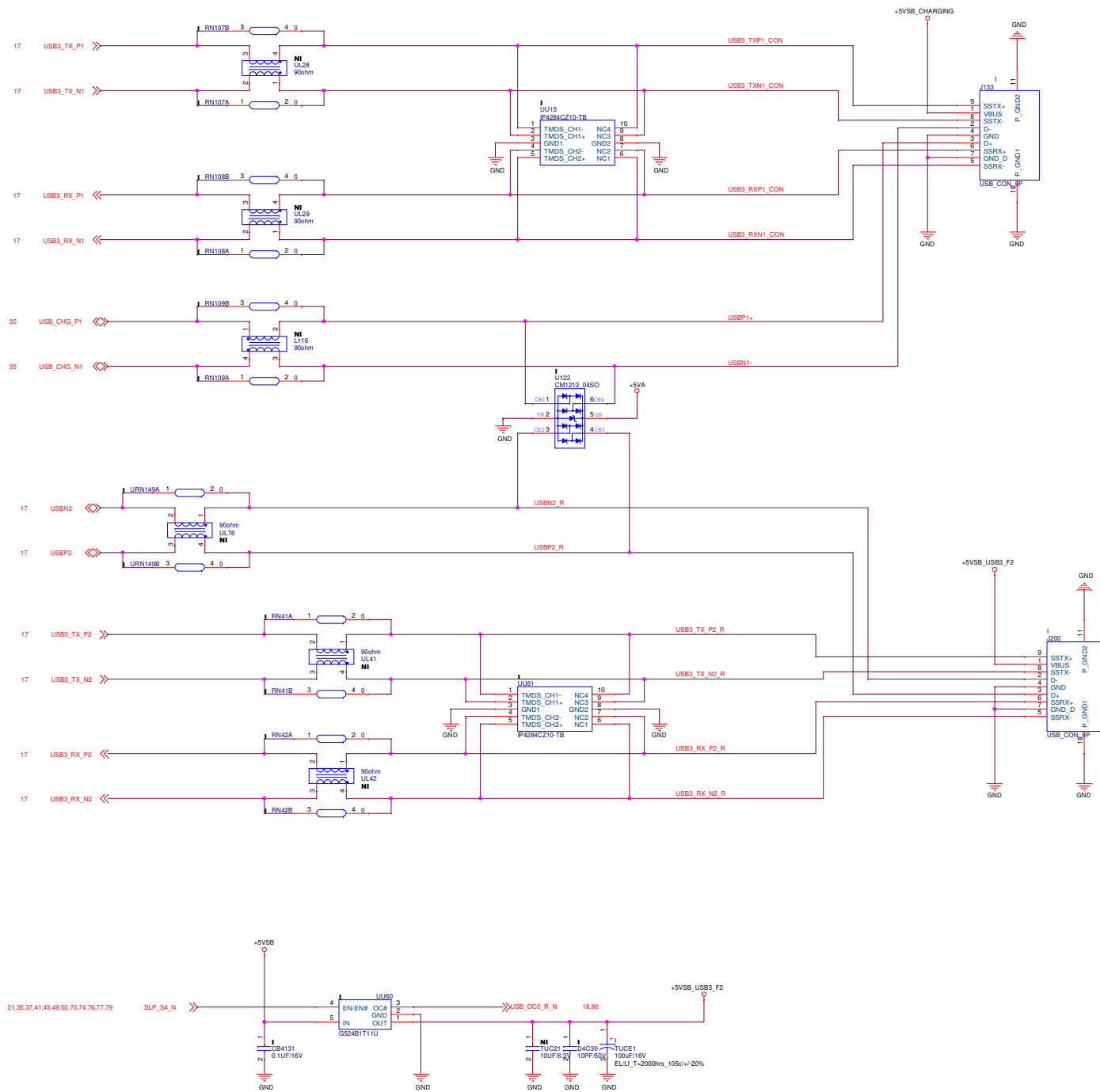






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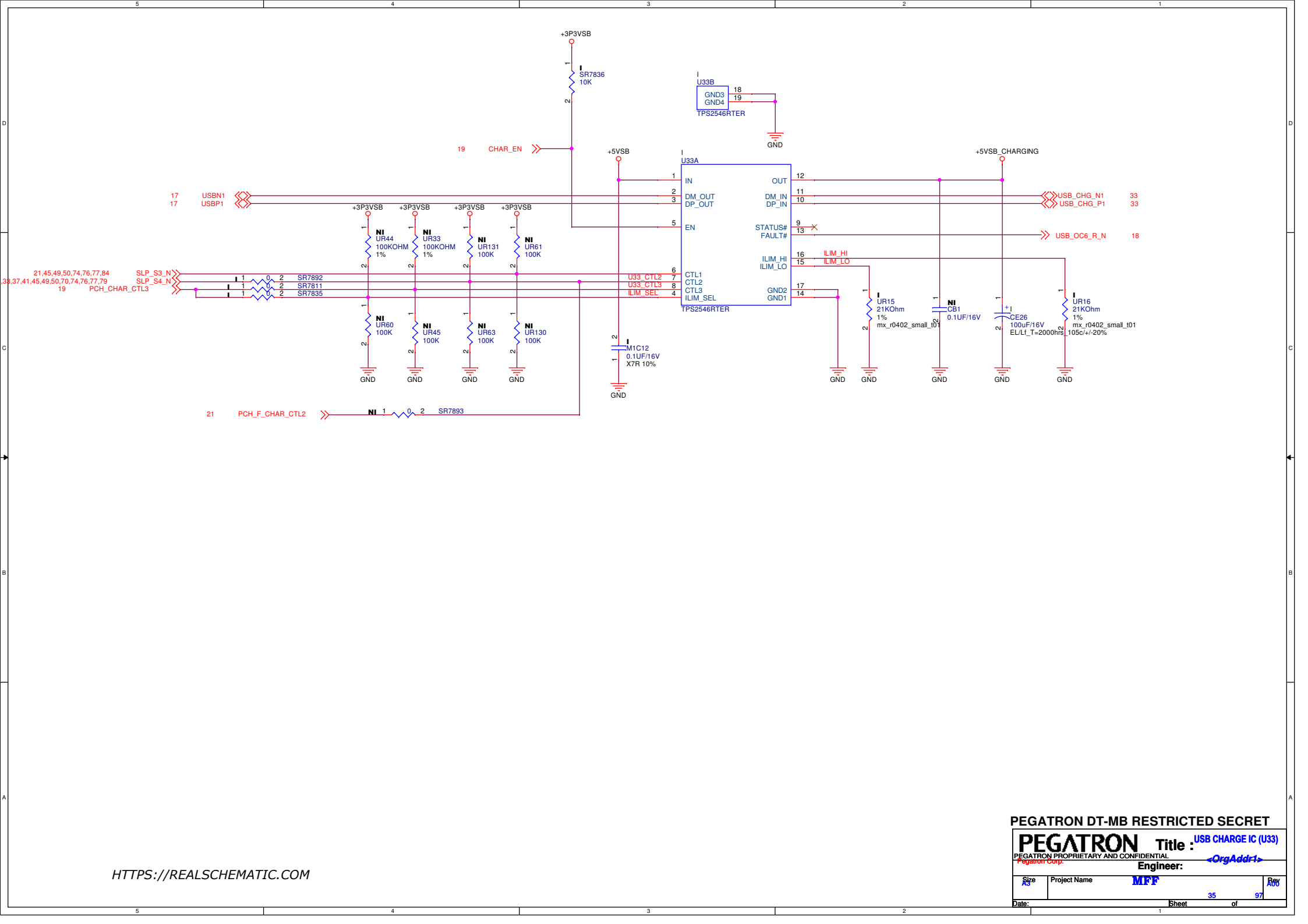


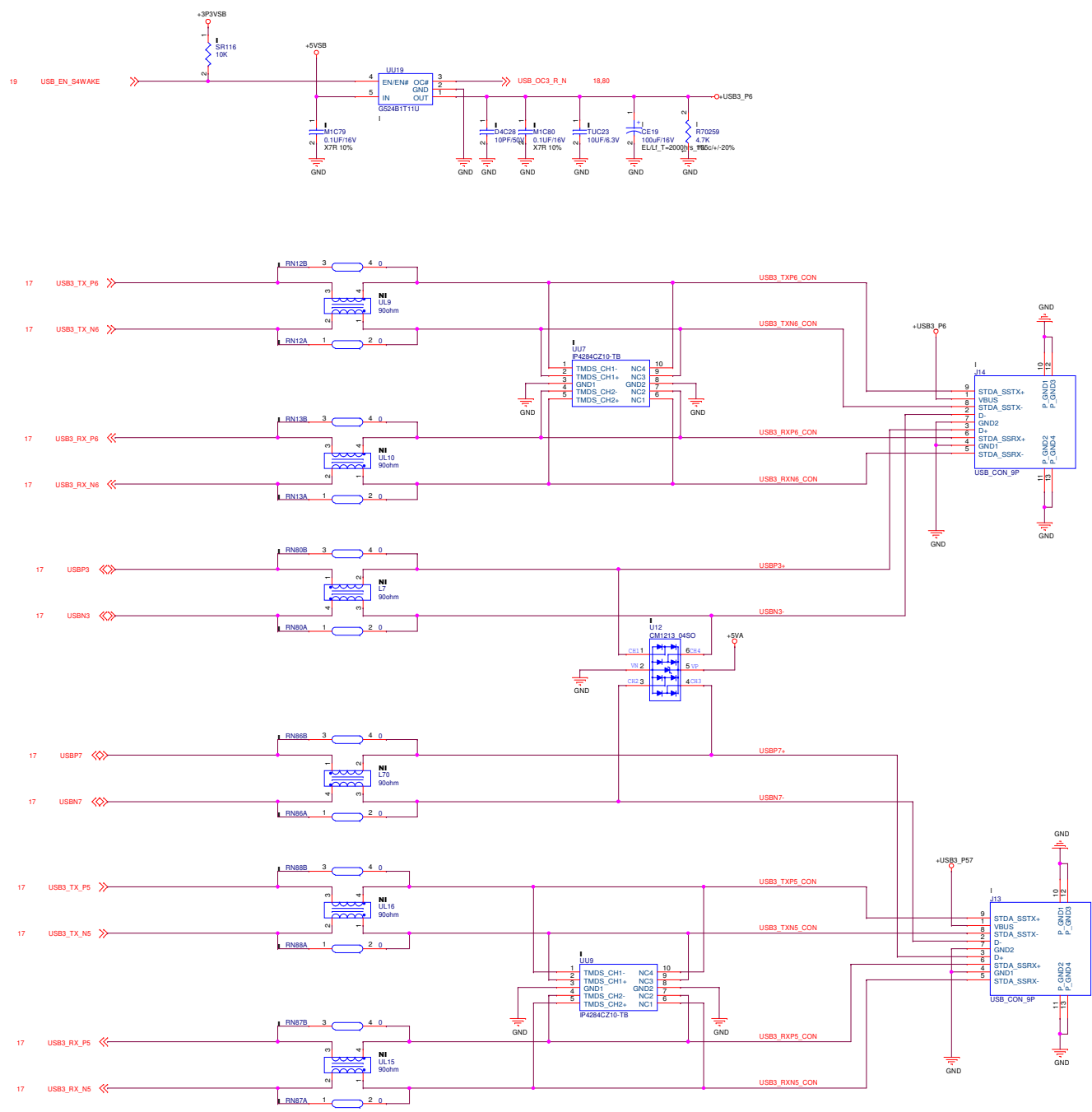
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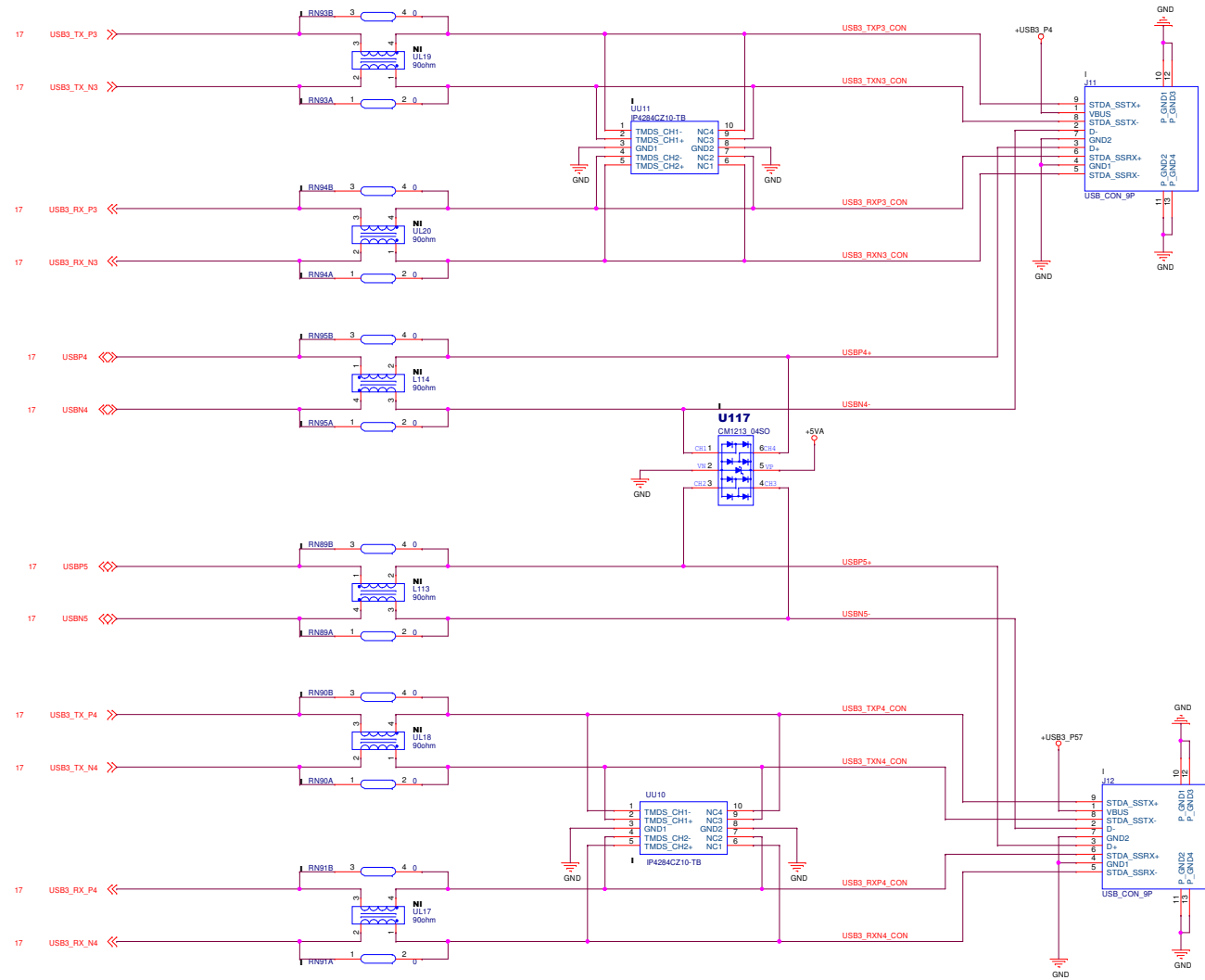
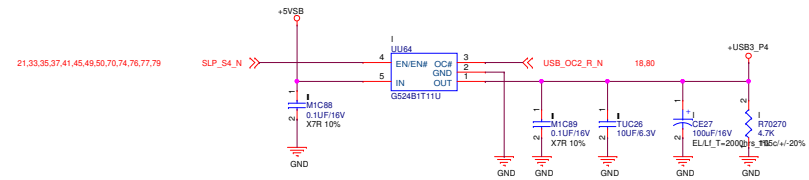
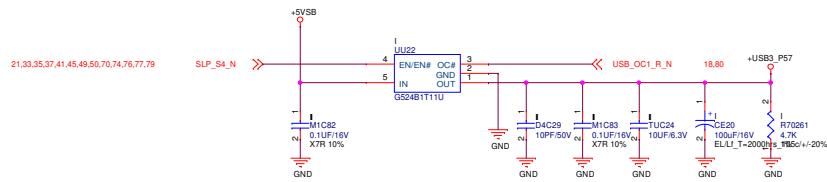
PEGATRON DT-MB RESTRICTED SECRET

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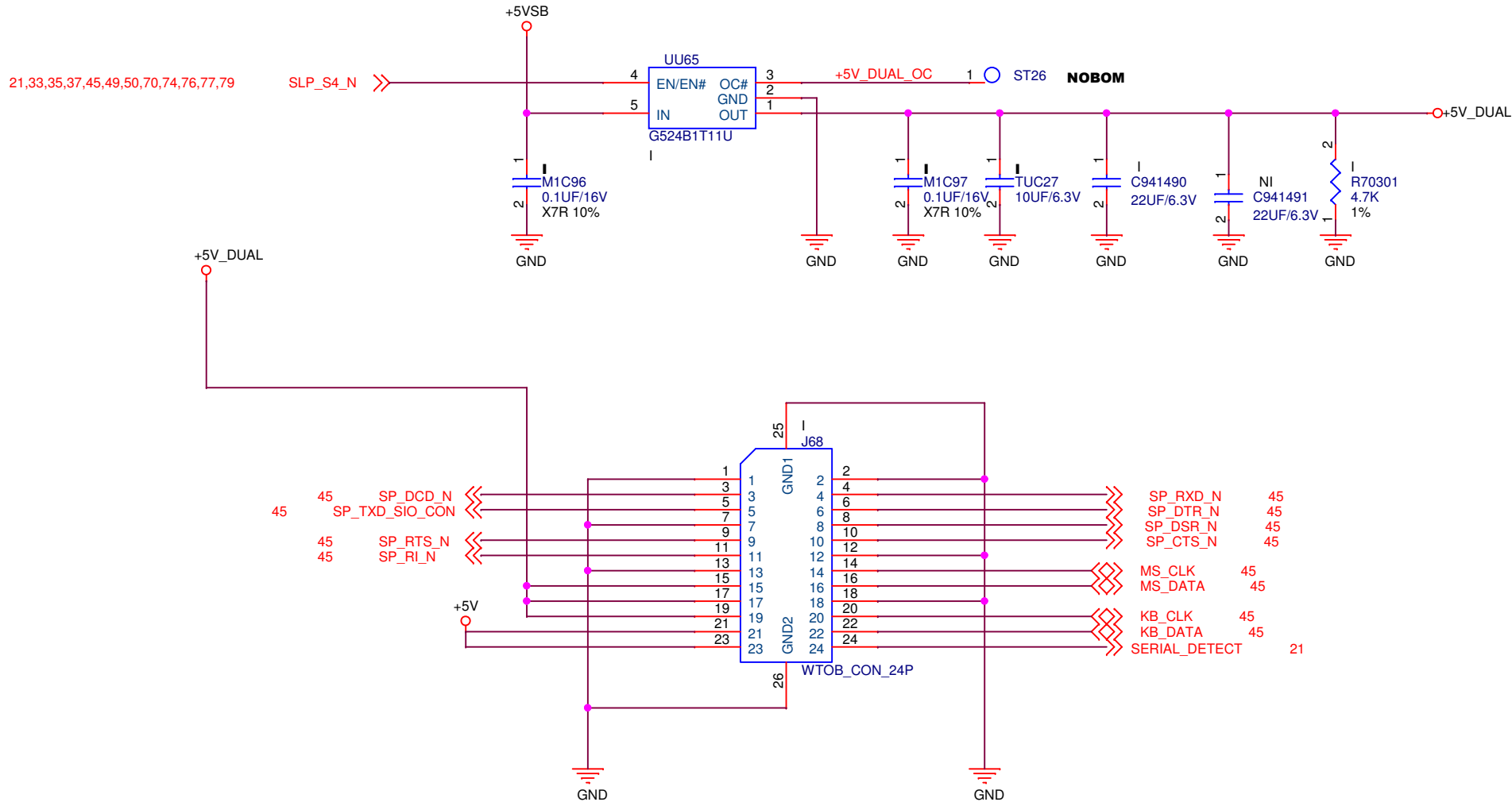
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PEGATRON PROPRIETARY AND CONFIDENTIAL		Front USB3.0	
PEGATRON Corp.		Engineer: <OrgAddri>	
Size	Project Name	Rev	Rev
U115	DT-MB	33	97
U115	DT-MB	33	97

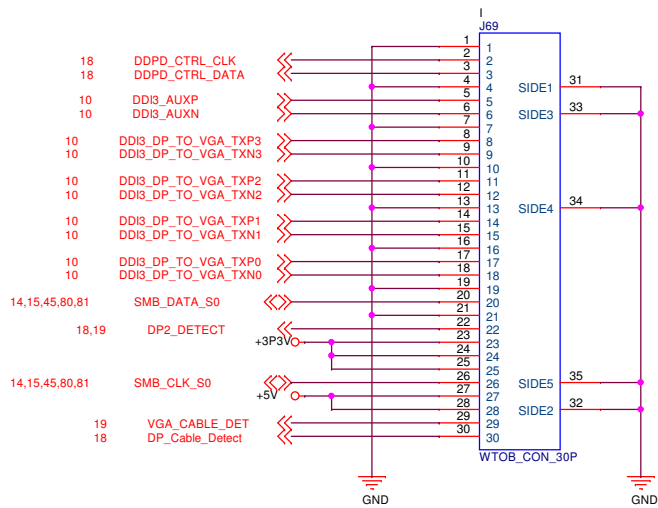


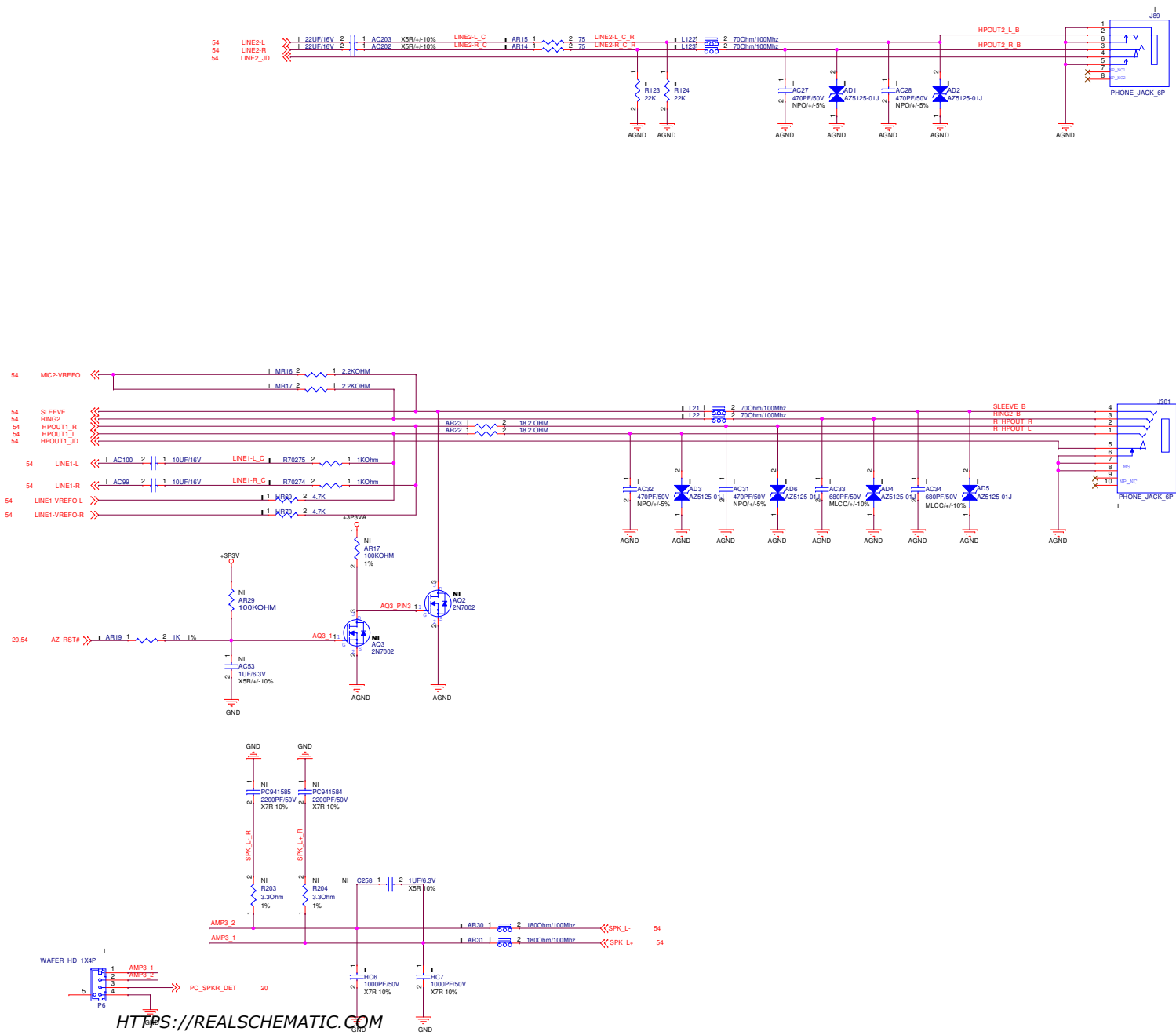




PEGATRON DT-MB RESTRICTED SECRET

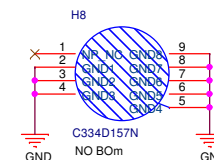
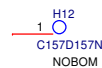
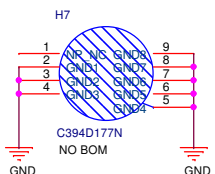
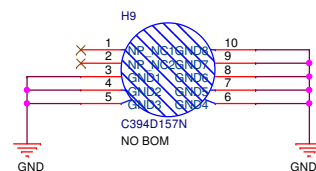
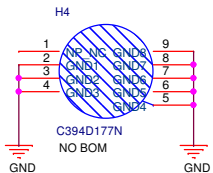
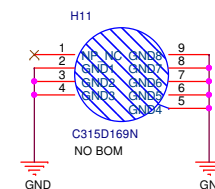
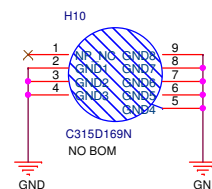
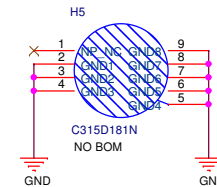
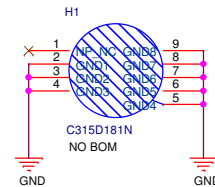
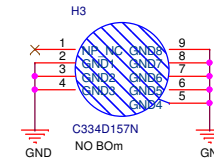
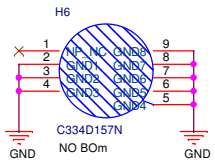






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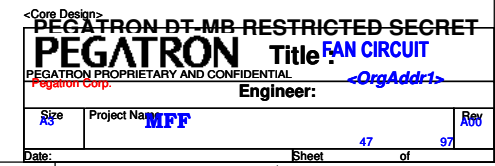
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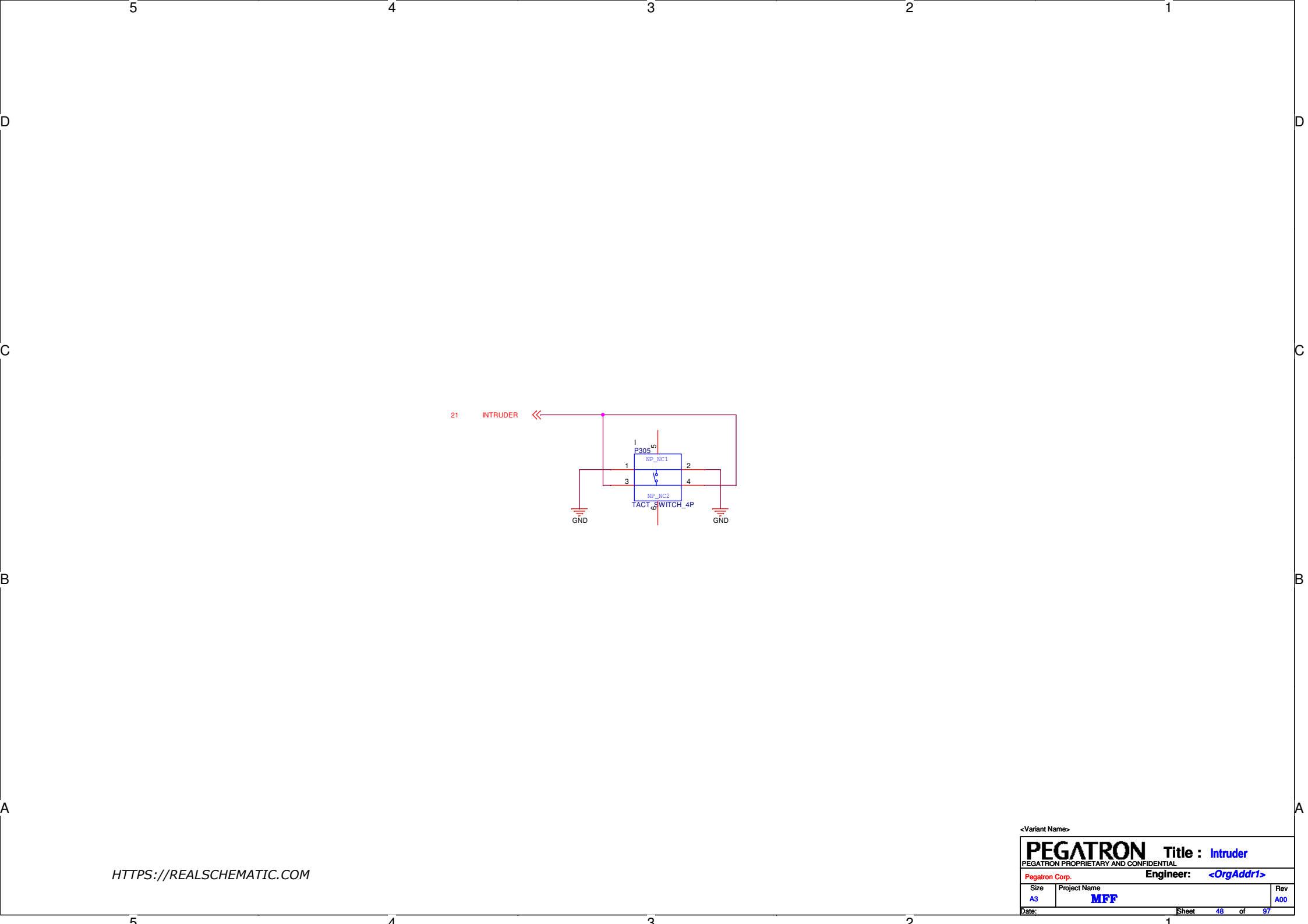
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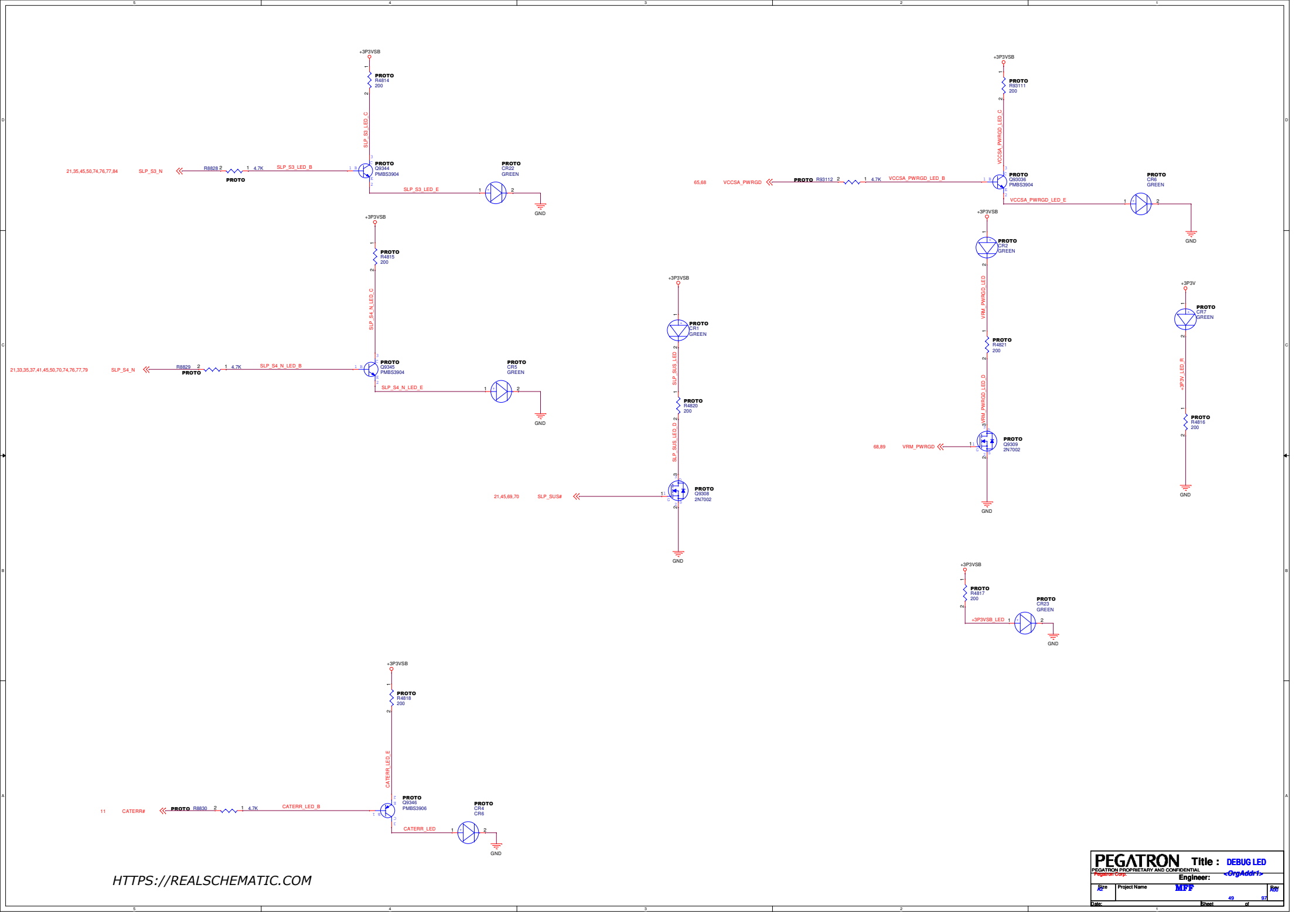
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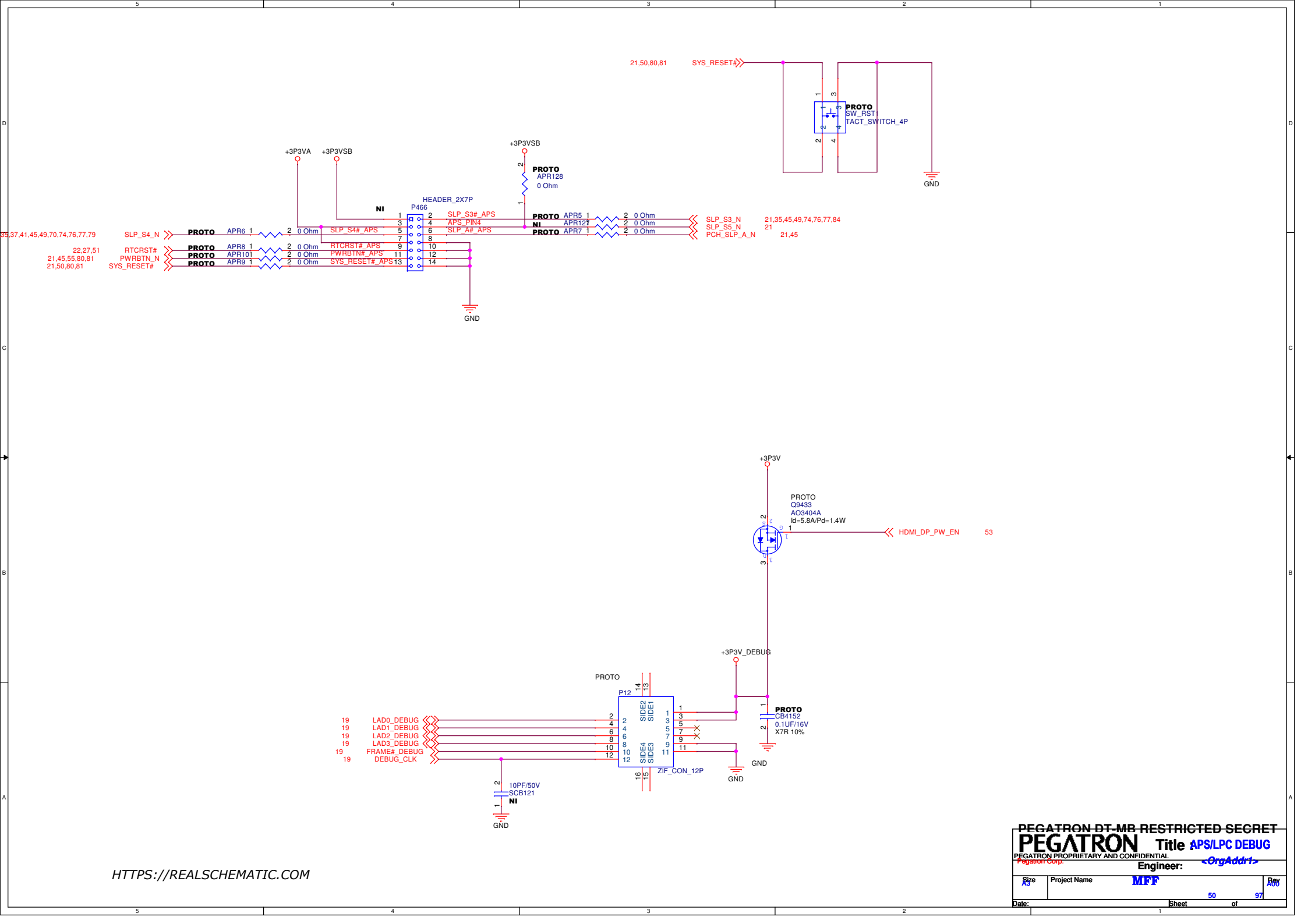
Pegatron Corp. Size A3 Project Name MFF Rev

Date: Sheet 46 of 97





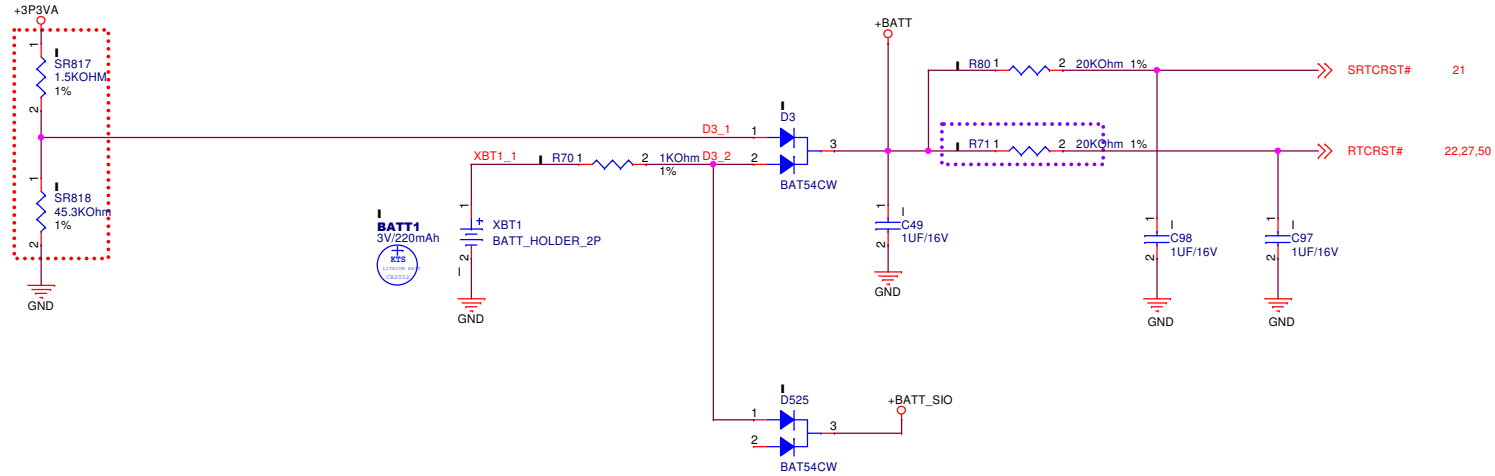


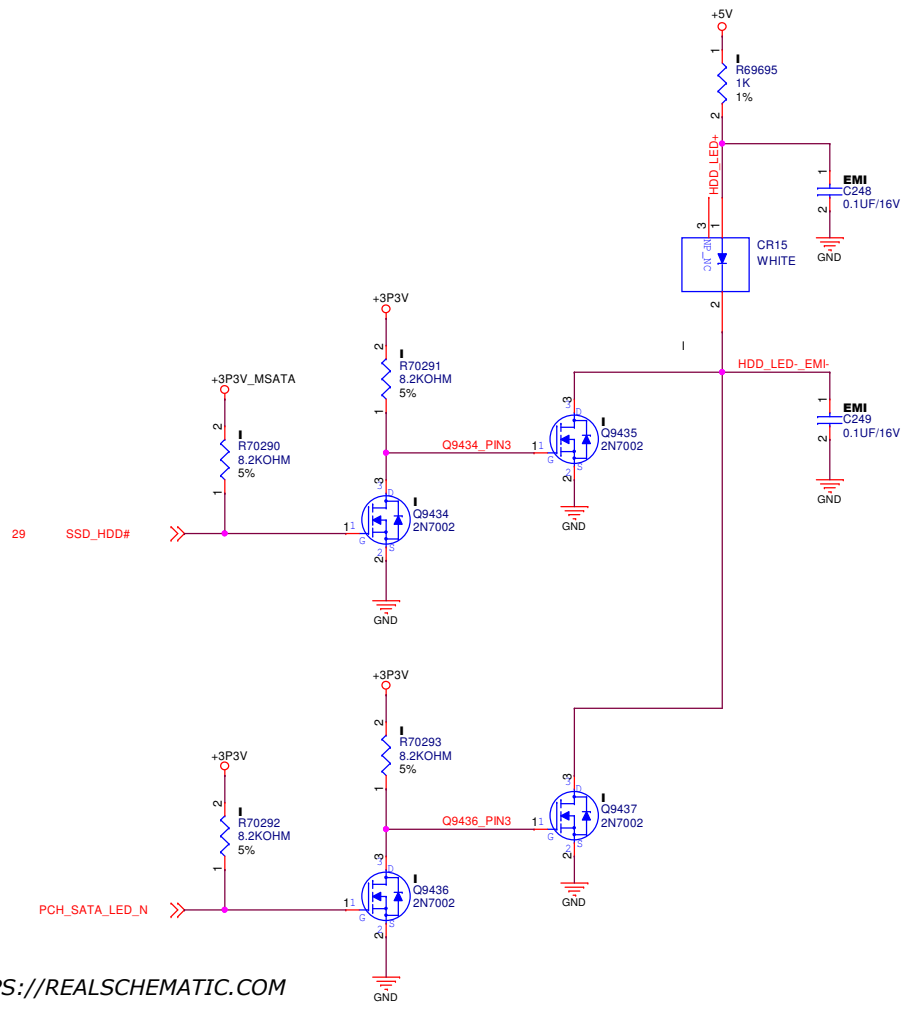
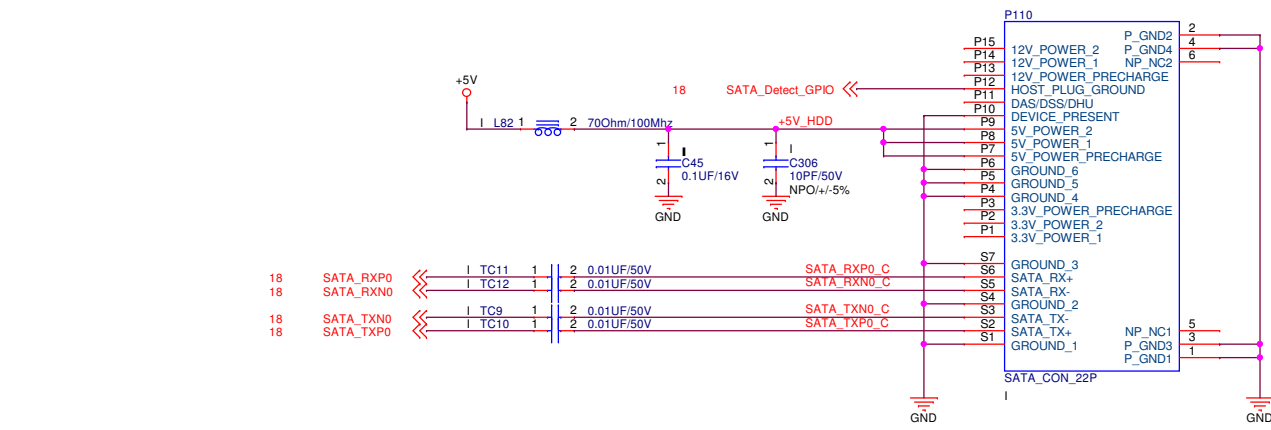


1103 by PDG p324
VCCDSW 3p3 to drop the voltage and meet the max
VCCRTC < 3.2V specification. The cost impact is small but
this solution will result in an ~0.25 mW power loss in
non-G3 state. In this solution, the dual diodes must be in a
single Si package to ensure matched Vf characteristics.
Initial resistor value recommendations are R2=1.5 KΩ and
R3=45 KΩ.

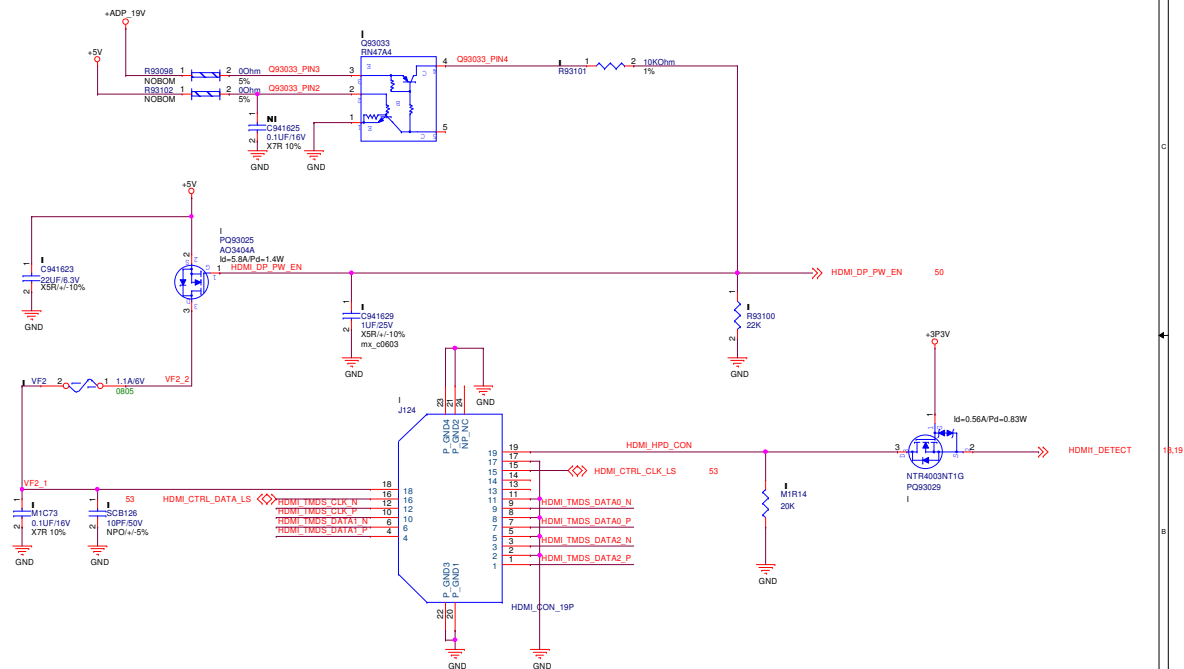
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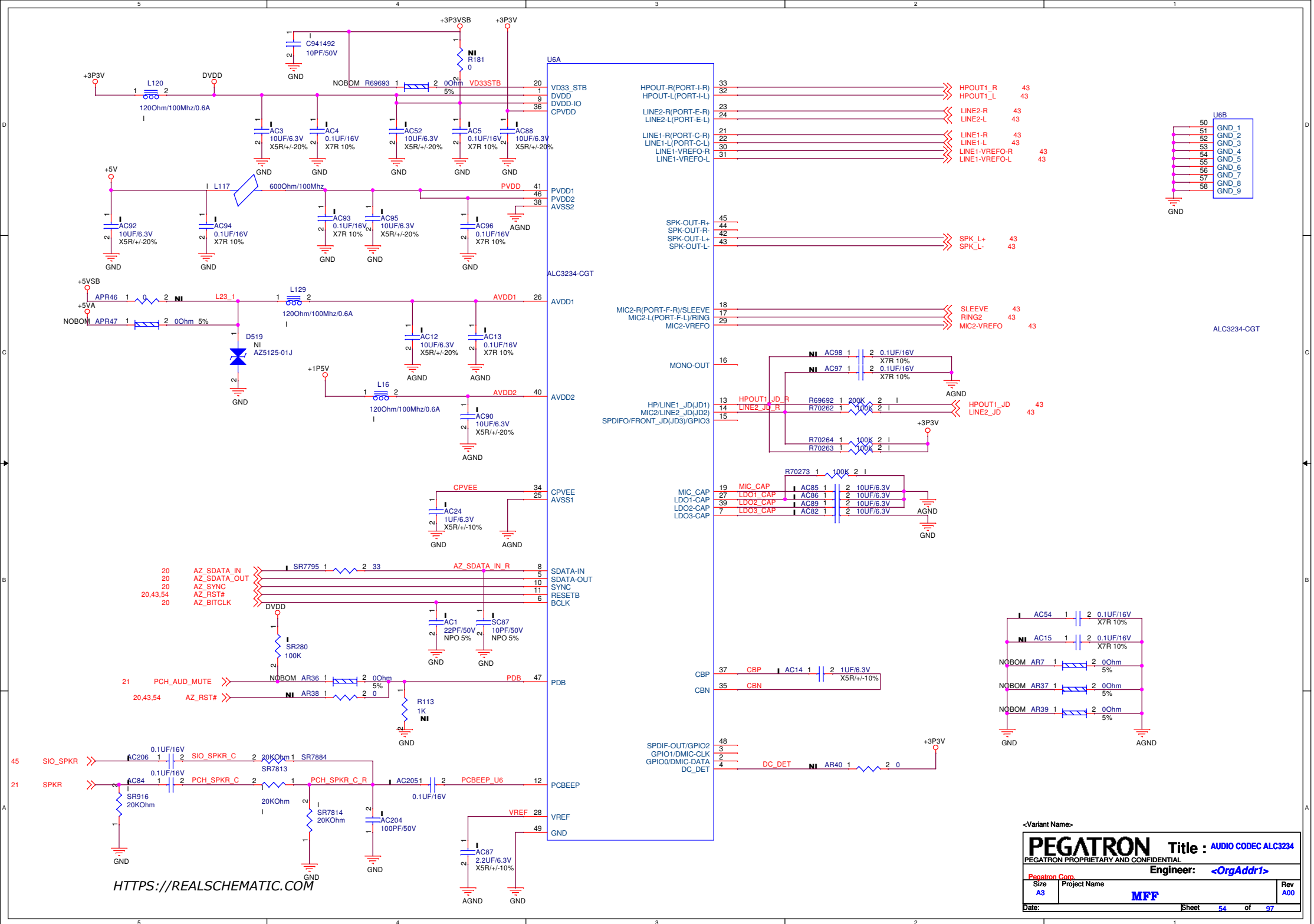
Original circuit design 27.4K(10X212274310)
Intel Sequence asked 20K 1%, CRB asked 30.1K.

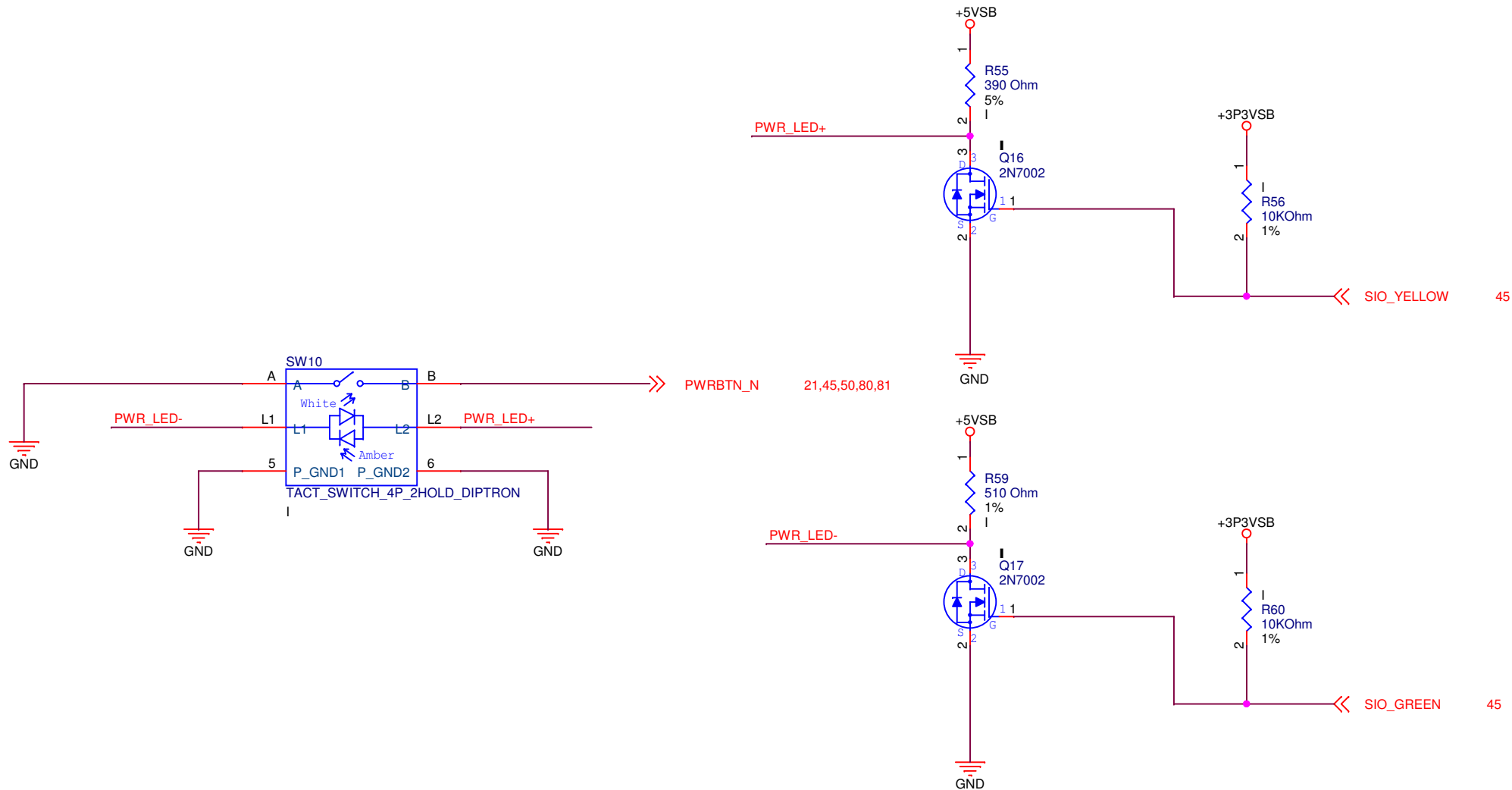




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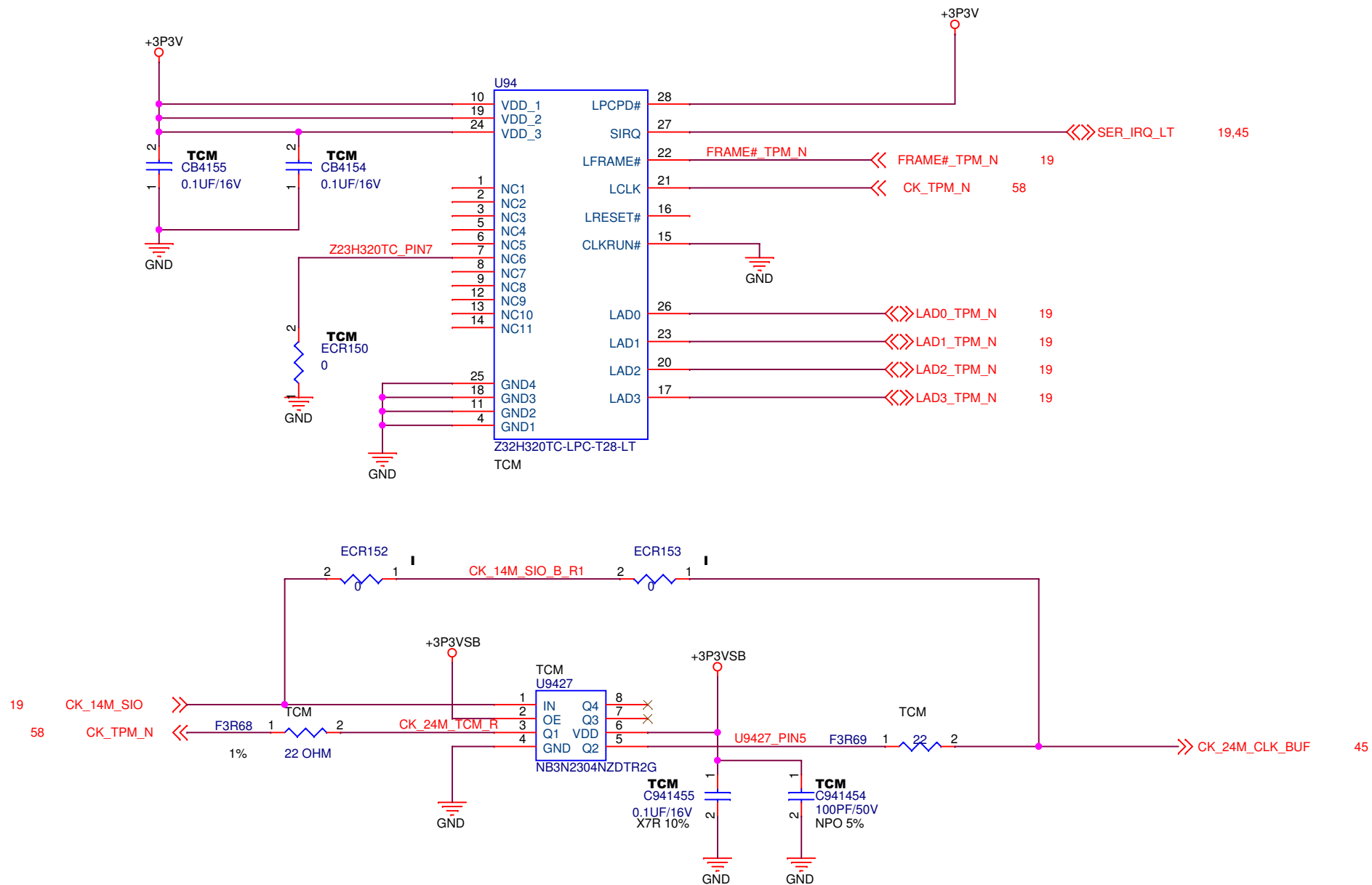






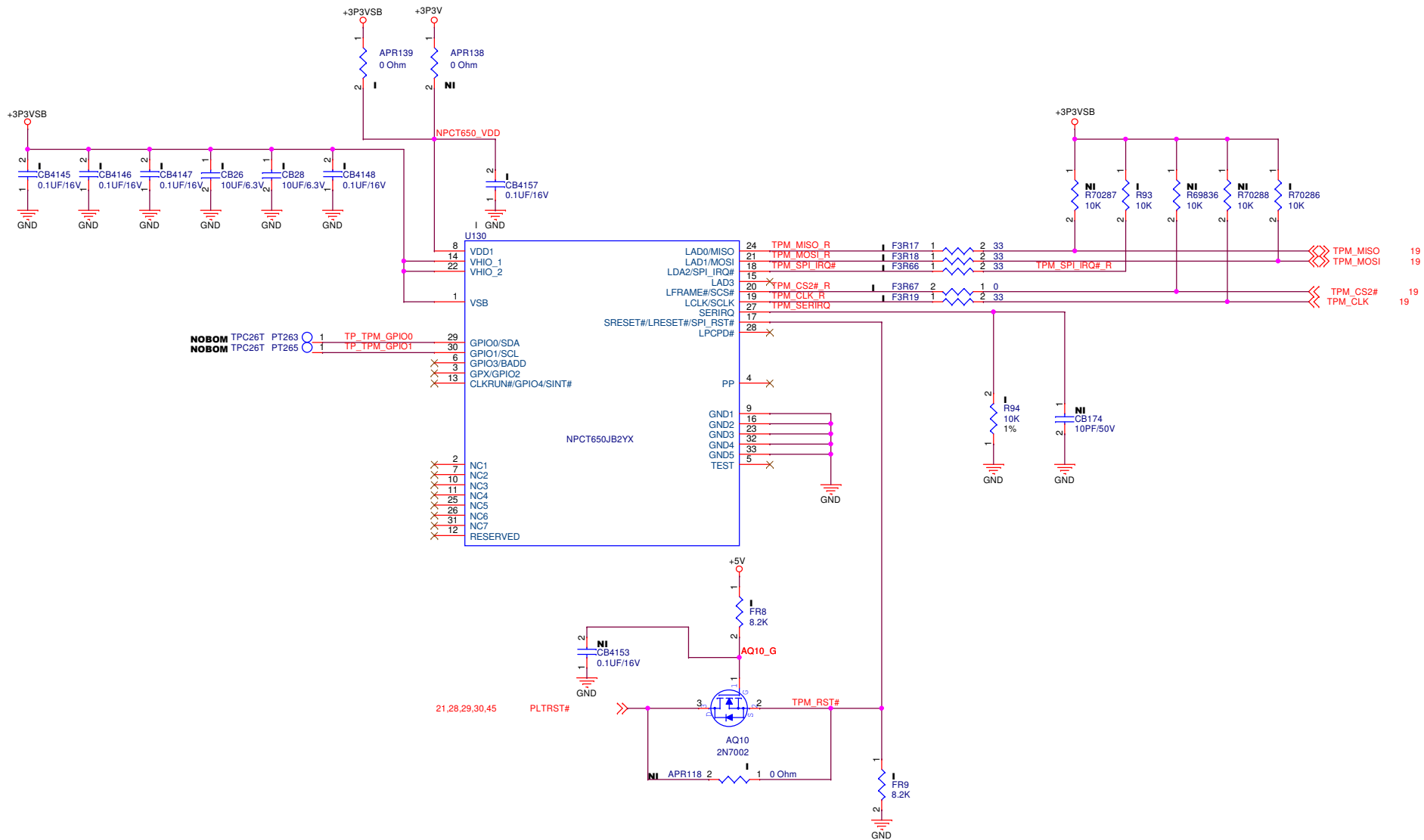
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
Pegatron Corp.		Engineer: <OrgAddr1>	
Size	Project Name	MFF	Rev
4x			
Date:		Sheet 55	of 97



PEGATRON DT-MB RESTRICTED SECRET
<Core Design>

PEGATRON		Title TPM_Z32H320TC	
PEGATRON PROPRIETARY AND CONFIDENTIAL		<OrgAddr1>	
Engineer:			
Size	Project Name	Rev	
RA	MFF	A00	
Date:		Sheet 58	of 97



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PEGATRON DT-MB RESTRICTED SECRET

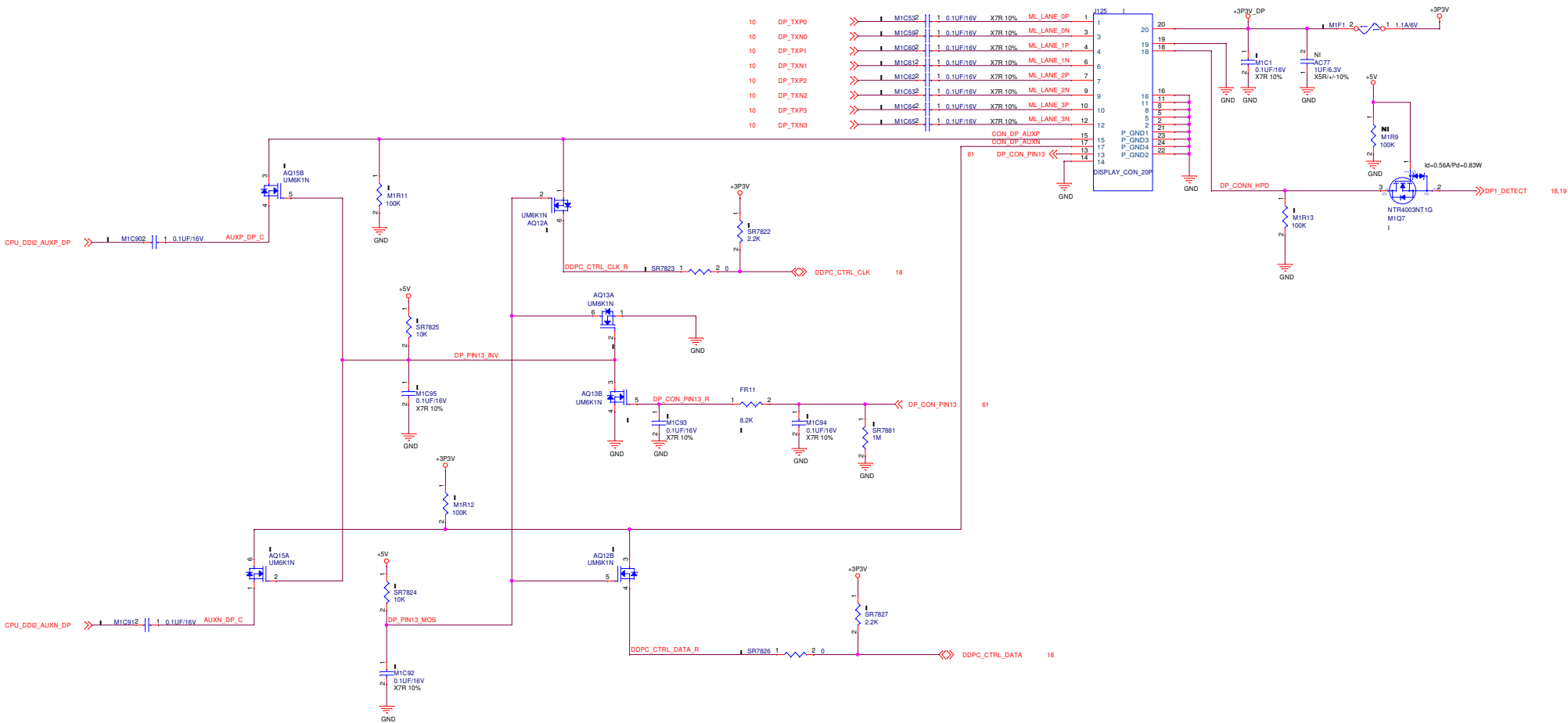
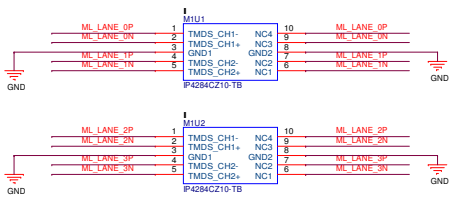
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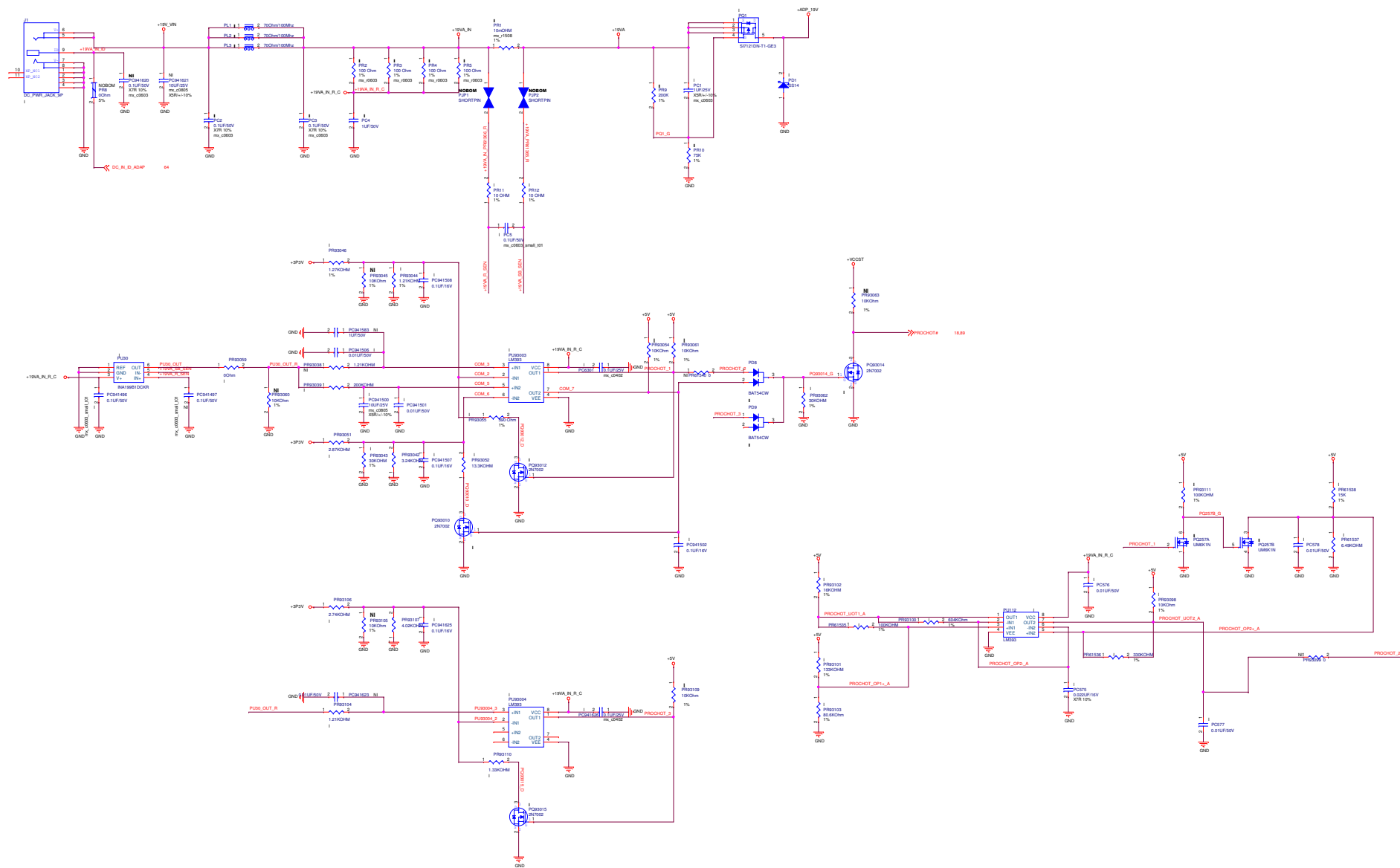
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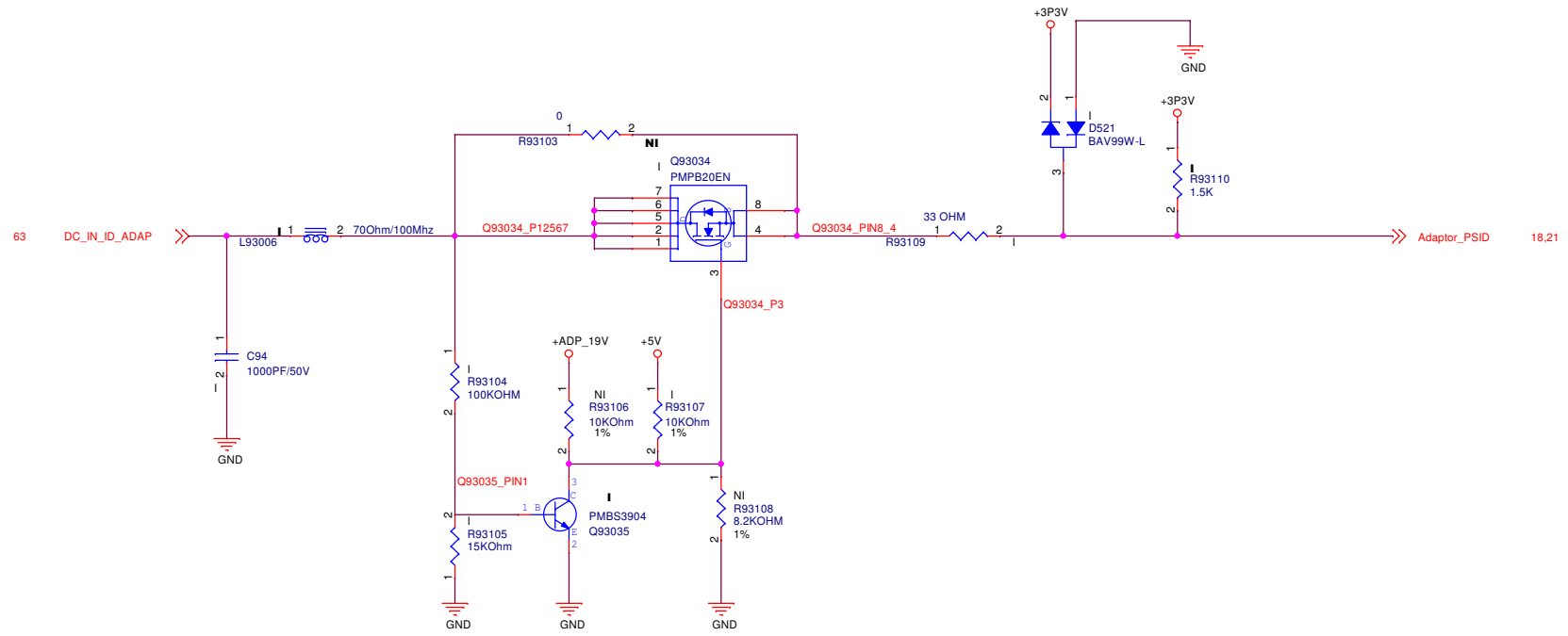
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Size	Project Name	Rev
A3	MFF	A00

Date: _____ Sheet 59 of 97





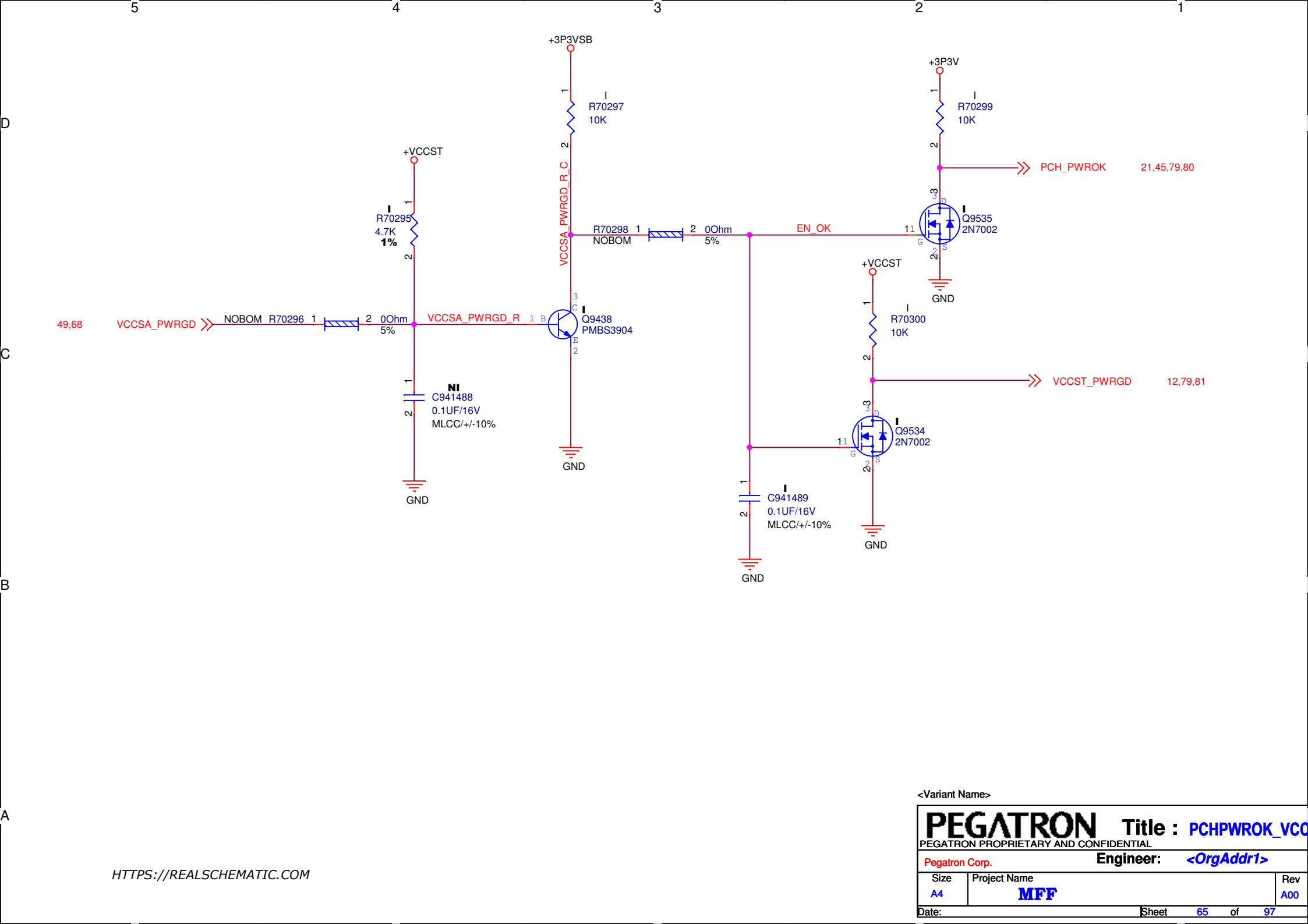


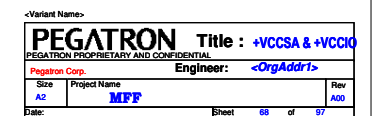
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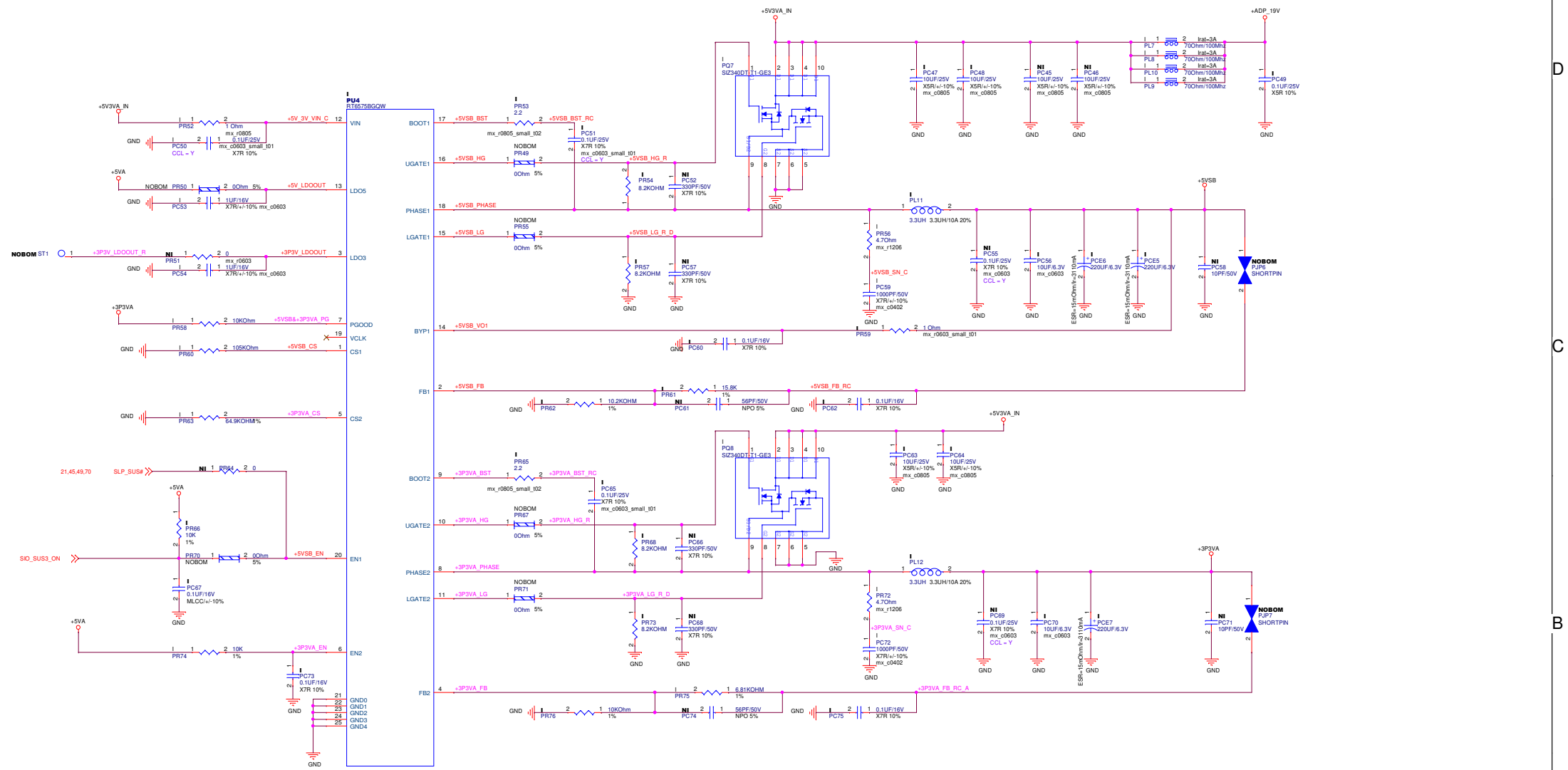
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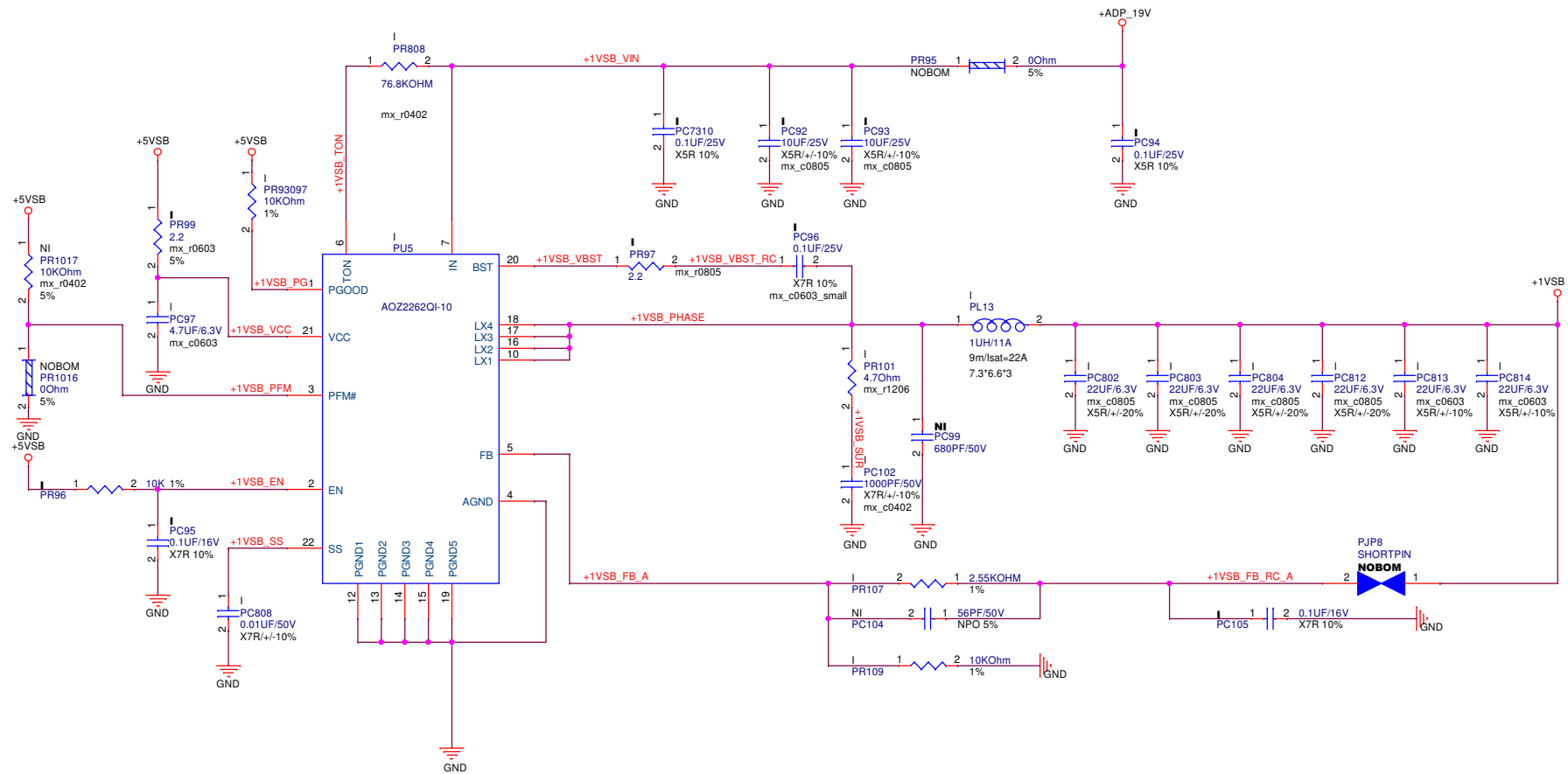
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Engineer: <OrgAddr1>	
Size A3	Project Name MFF
Date:	Rev A00

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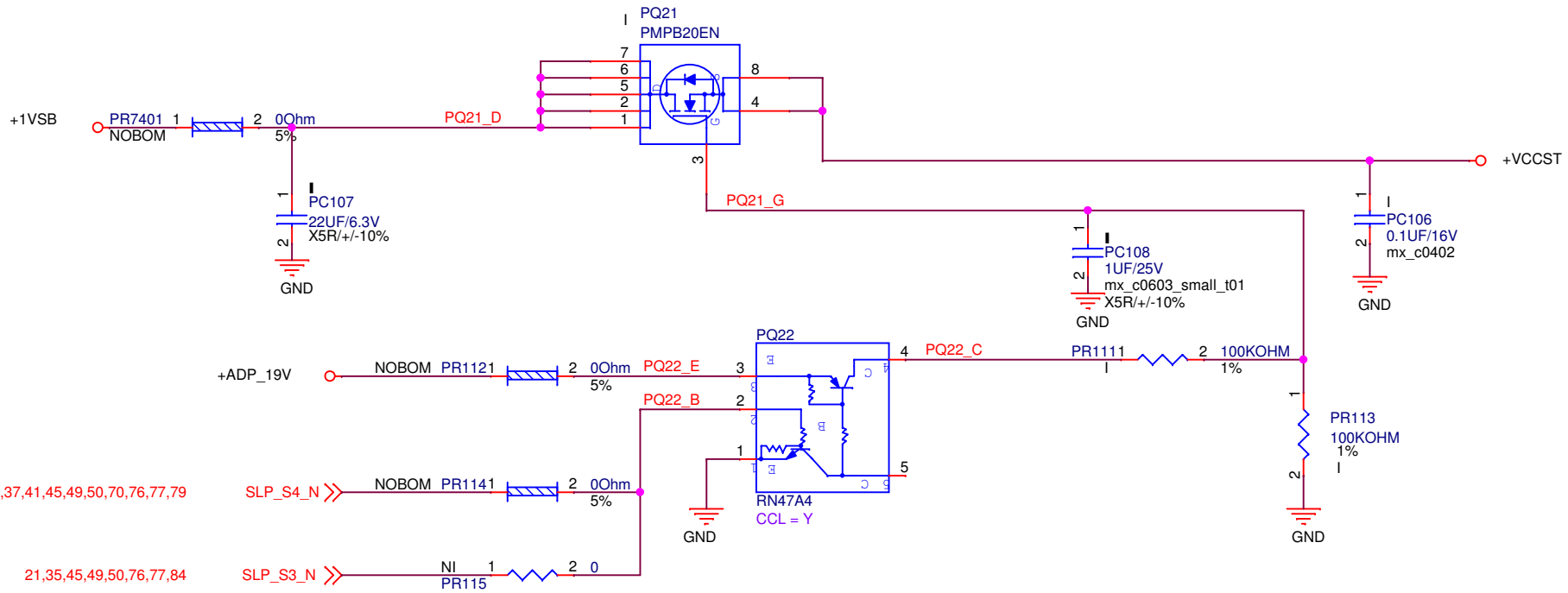
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
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Size A3	Project Name MFF	Rev A00	
Date:	Sheet 73 of 97		

D

C

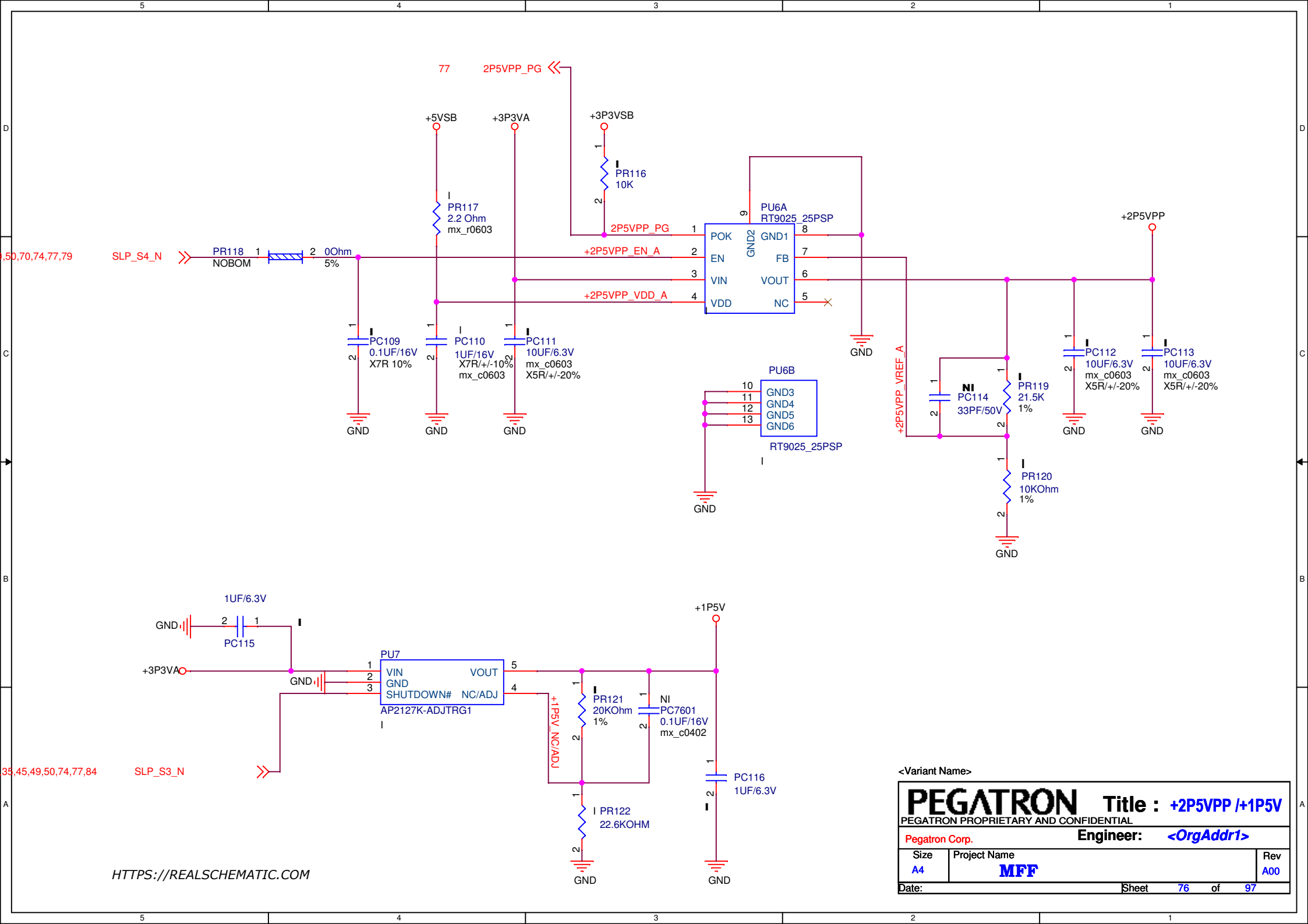
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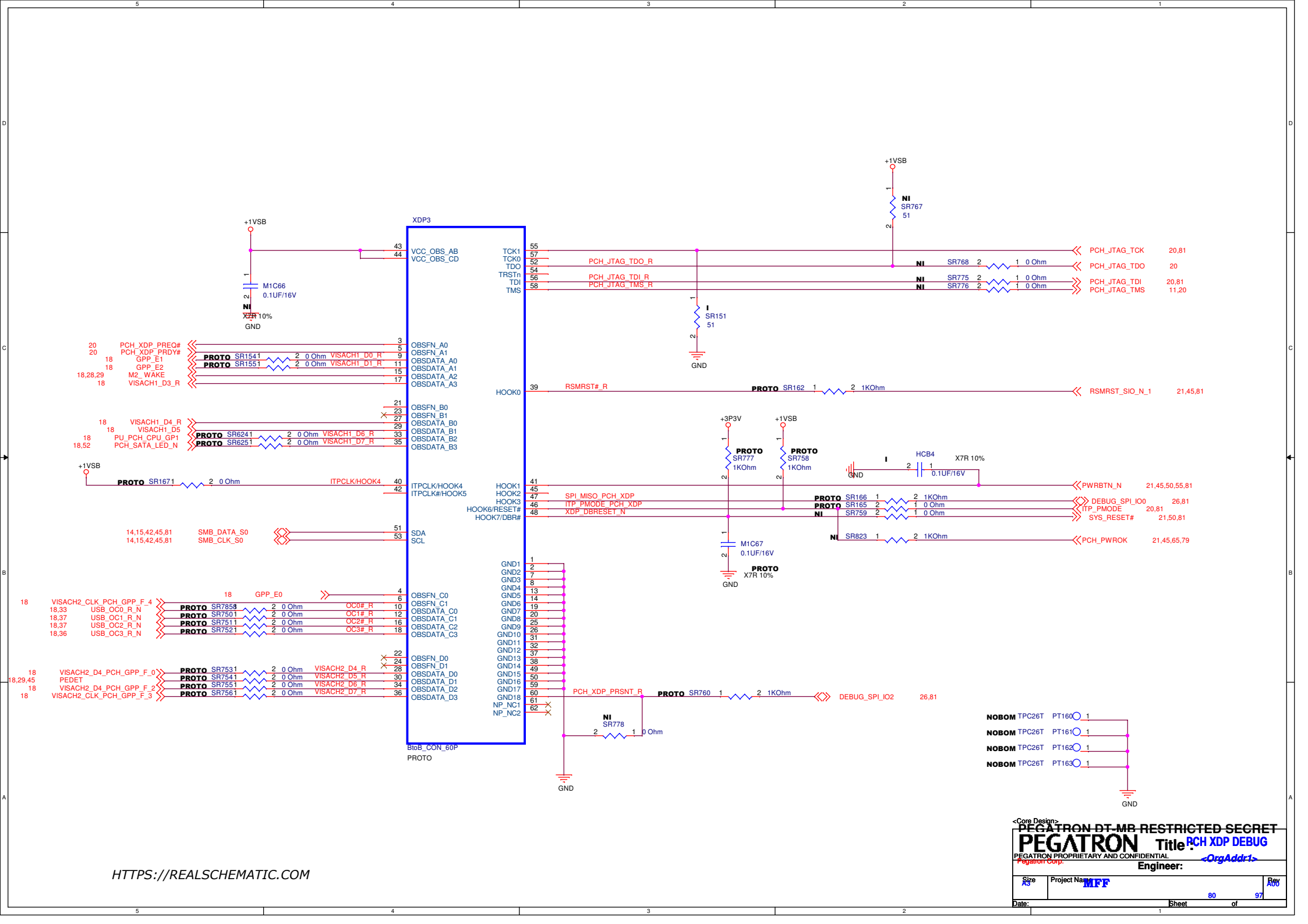
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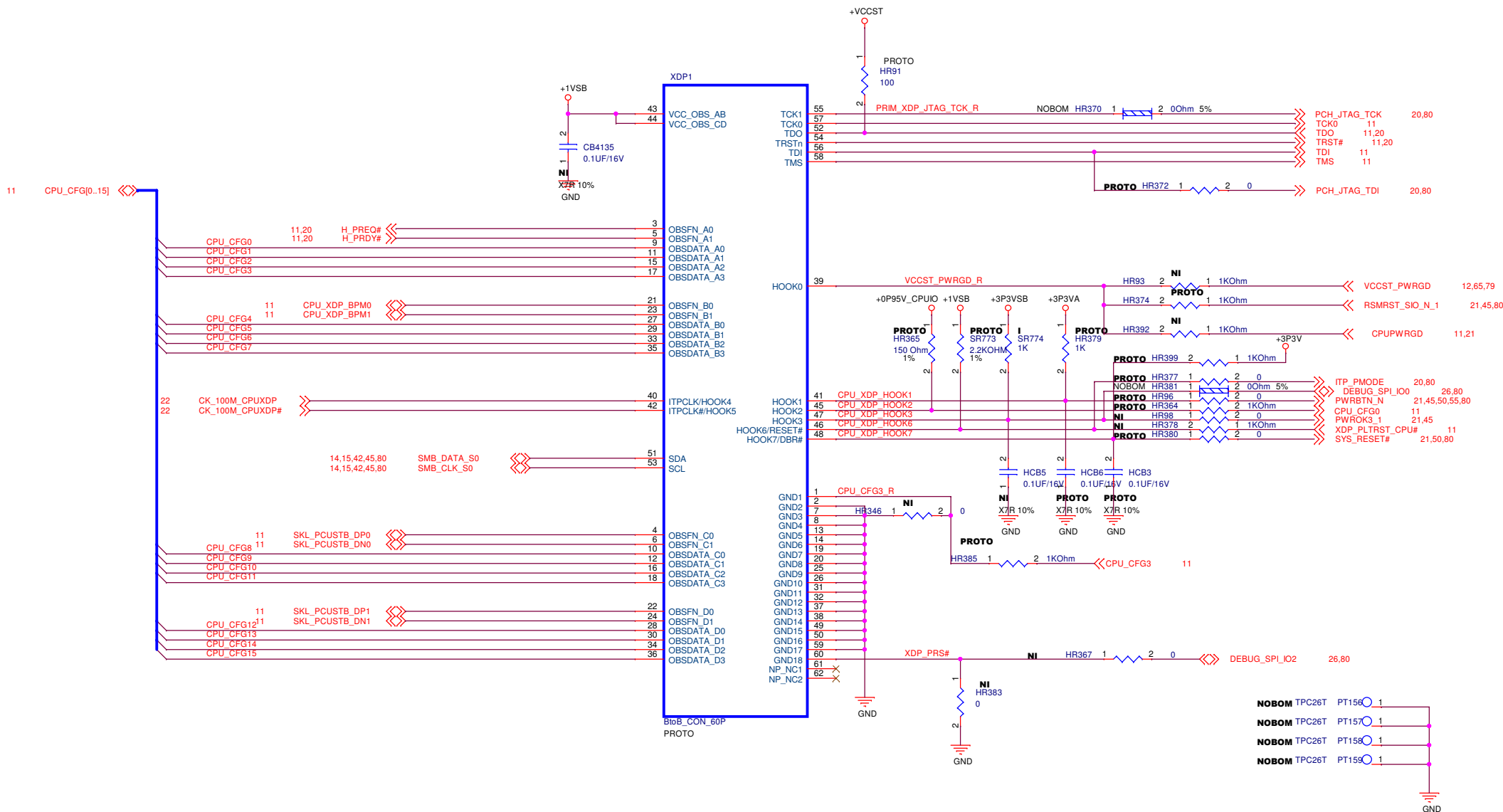
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Size A4	Project Name MFF		Rev A00
Date:	Sheet	74	of 97

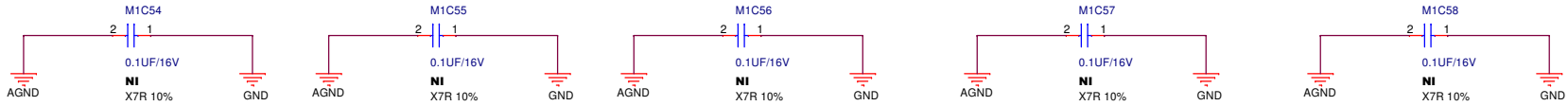


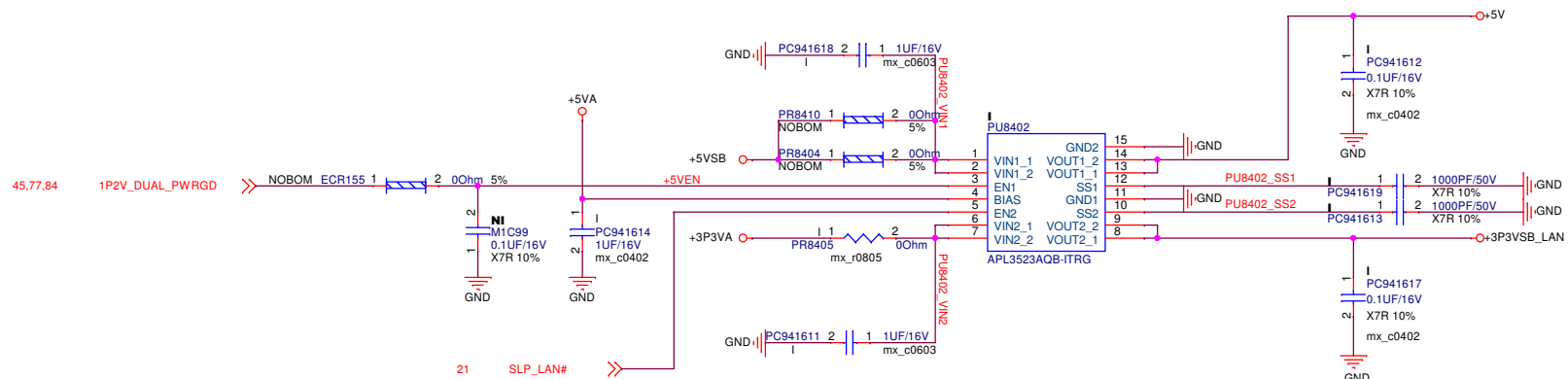
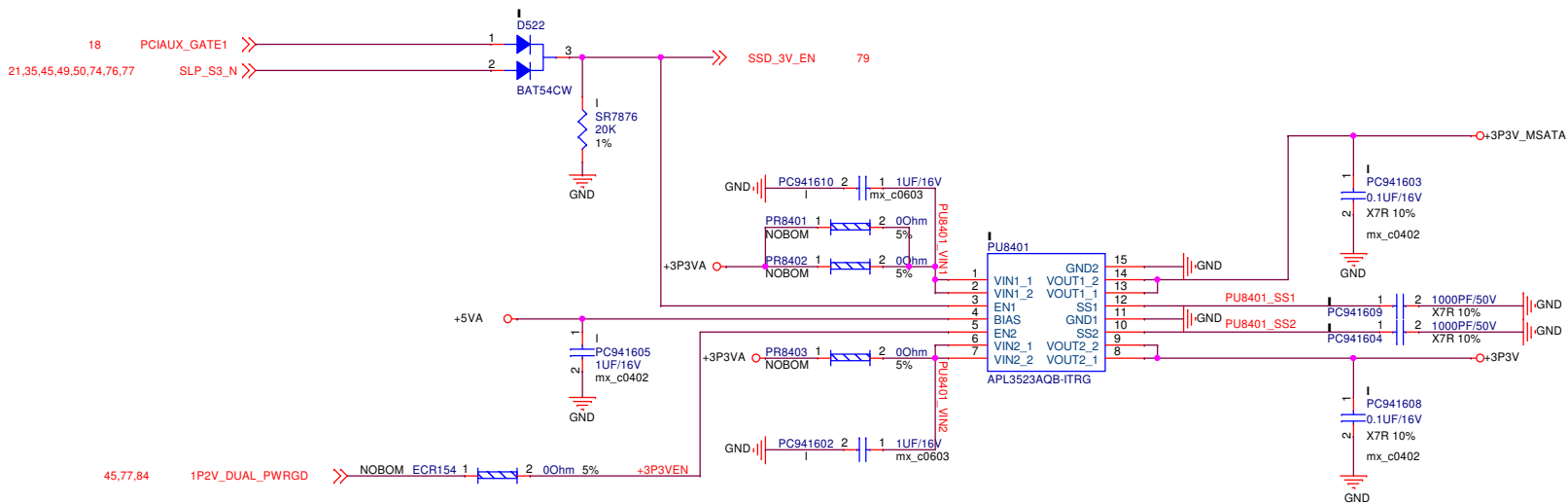
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Size	Project Name		Rev
A4	MFF		A00
Date:		Sheet	76 of 97

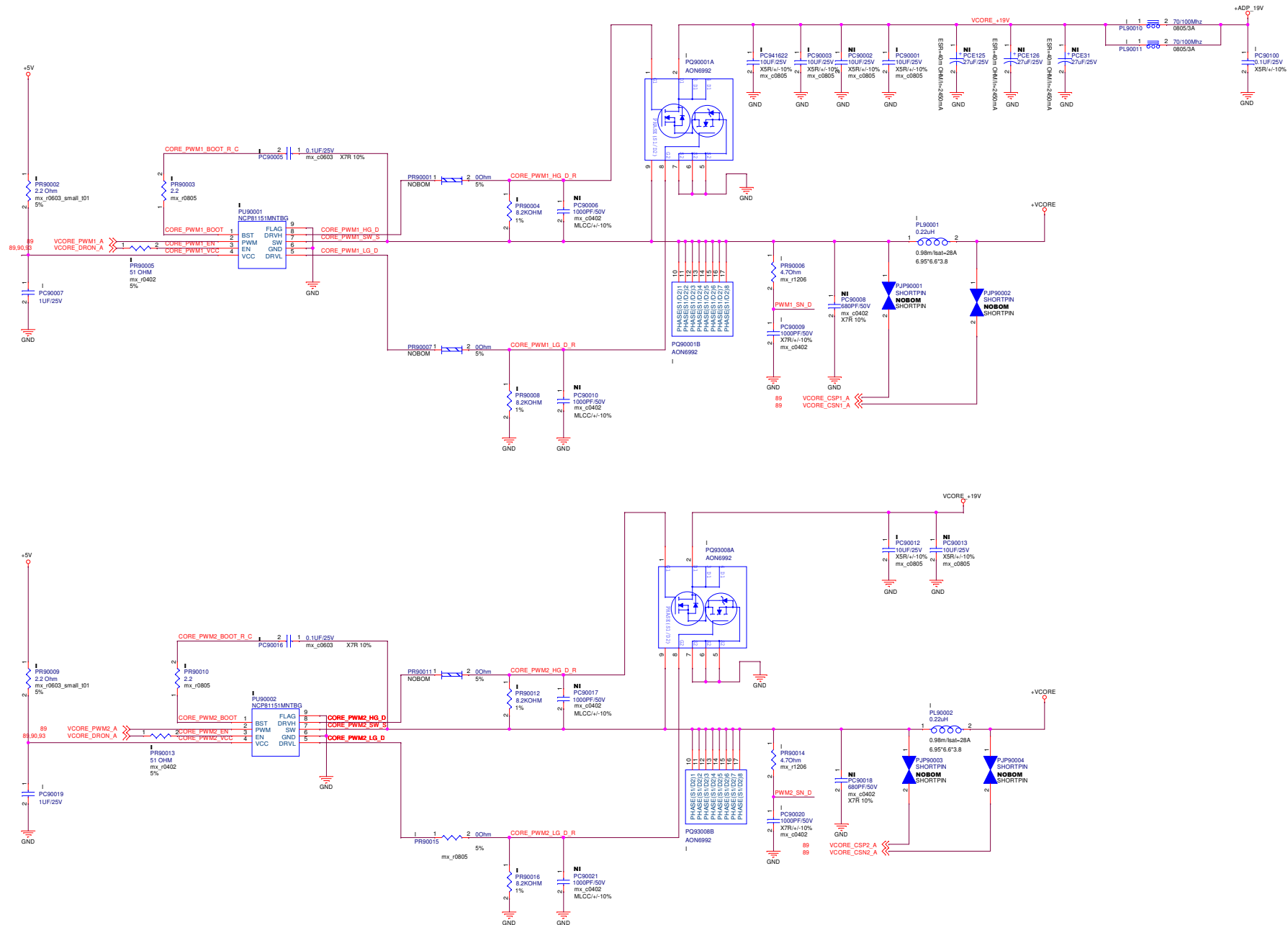


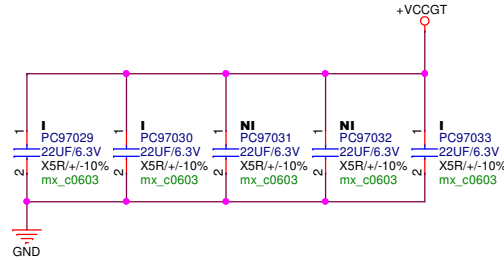
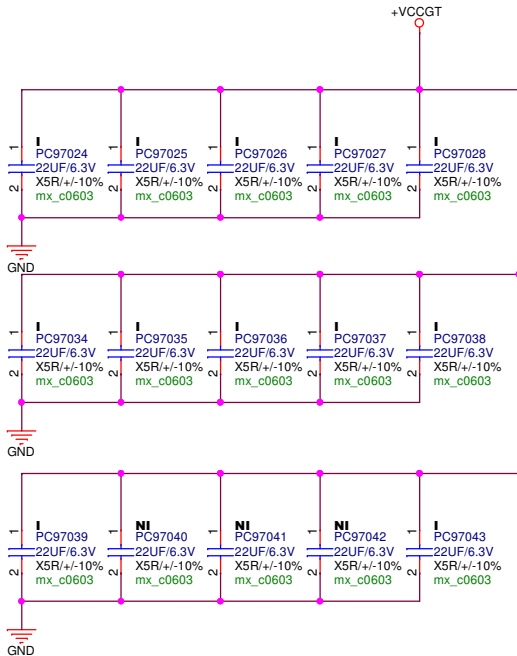
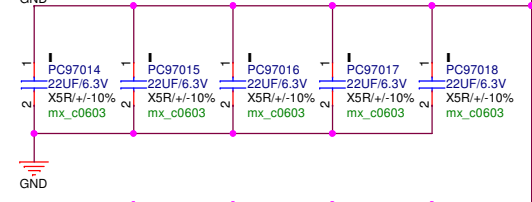
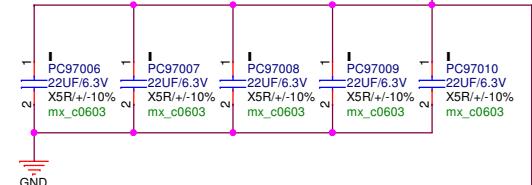
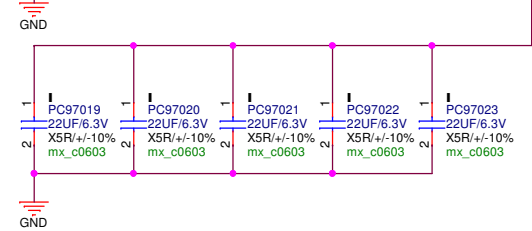
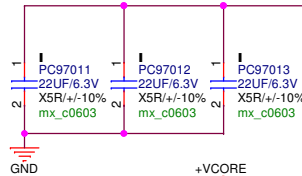
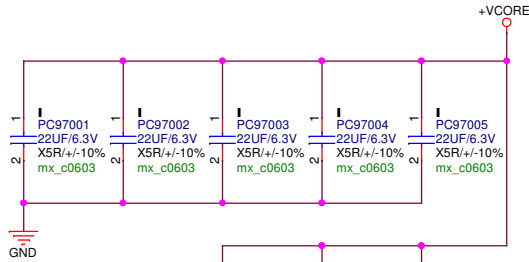
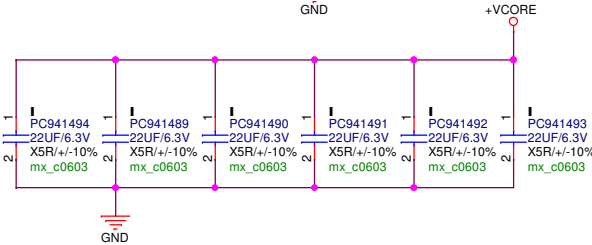
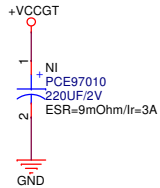
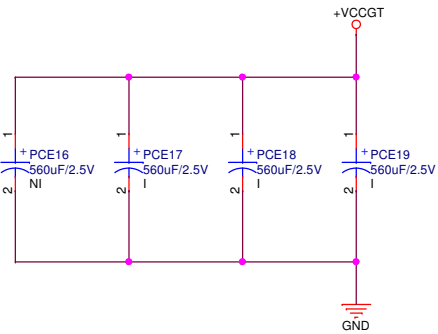
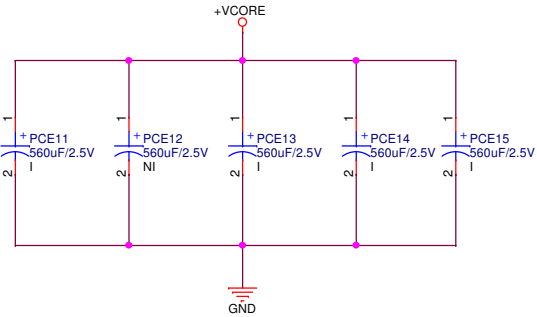






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<Variant Name>

PEGATRON Title : CORE & VCC_GT CAP
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Pegatron Corp. Engineer: <OrgAddr>

Size	Project Name	Rev
Custom	MFF	A00

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